FIG. 1

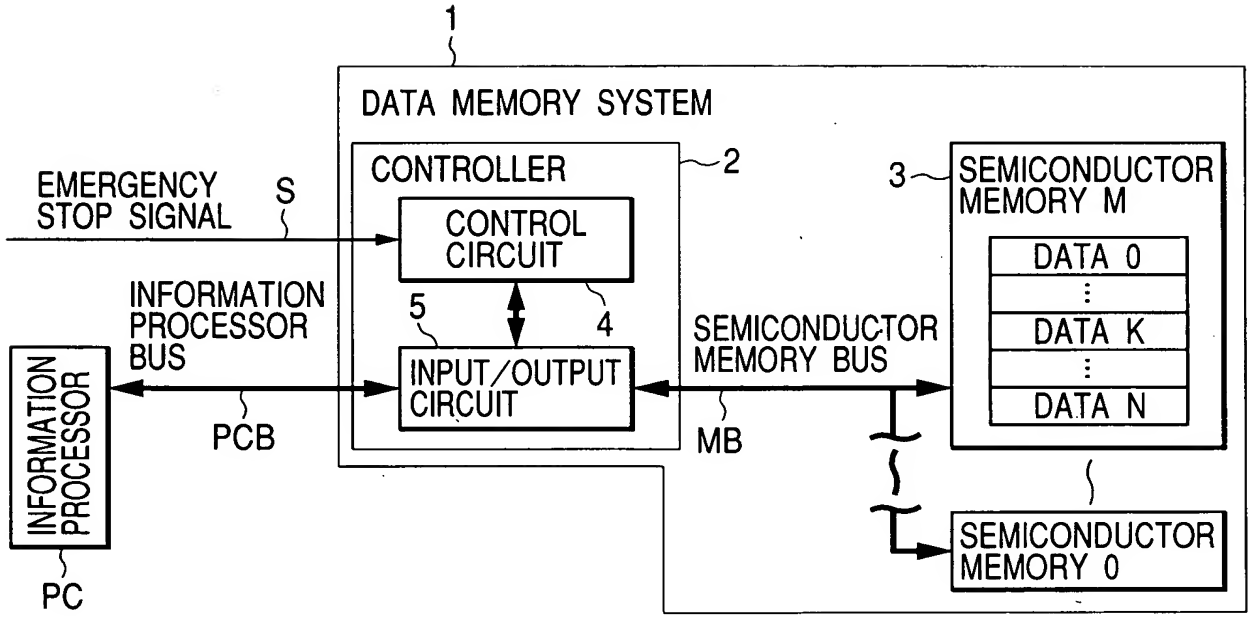

1
DATA MEMORY SYSTEM
CONTROLLER
2
CONTROL CIRCUIT
5
4
INPUT/OUTPUT CIRCUIT
EMERGENCY STOP SIGNAL
S
INFORMATION PROCESSOR BUS
PCB
INFORMATION PROCESSOR
PC
SEMICONDUCTOR MEMORY BUS
MB
3
SEMICONDUCTOR MEMORY M
DATA 0
DATA K
DATA N
SEMICONDUCTOR MEMORY 0

FIG. 2

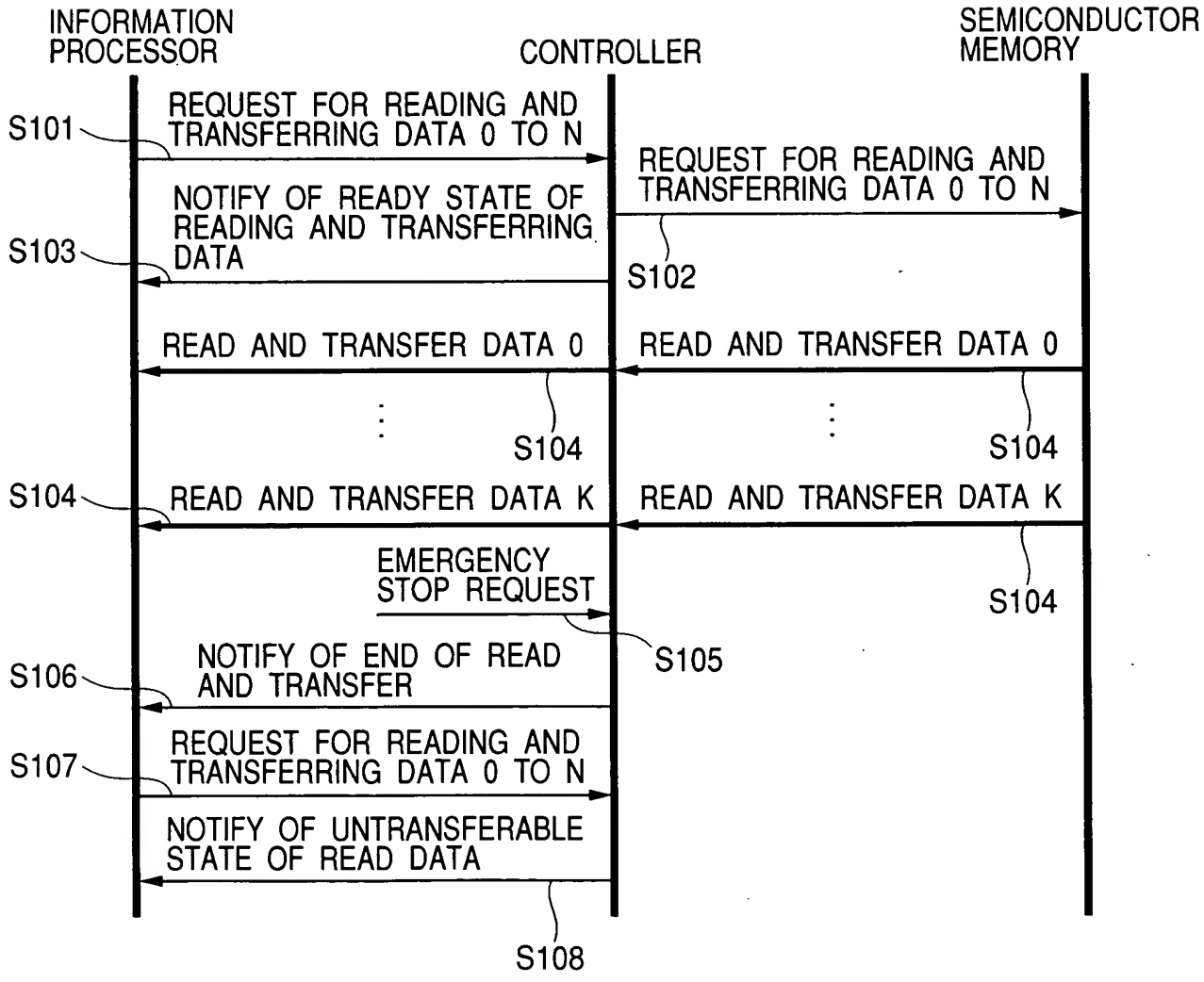

INFORMATION PROCESSOR
CONTROLLER
SEMICONDUCTOR MEMORY
S101
REQUEST FOR READING AND TRANSFERRING DATA 0 TO N
REQUEST FOR READING AND TRANSFERRING DATA 0 TO N
S102
S103
NOTIFY OF READY STATE OF READING AND TRANSFERRING DATA
READ AND TRANSFER DATA 0
READ AND TRANSFER DATA 0
S104
S104
S104
READ AND TRANSFER DATA K
READ AND TRANSFER DATA K
S104
EMERGENCY STOP REQUEST
S105
S106
NOTIFY OF END OF READ AND TRANSFER
S107
REQUEST FOR READING AND TRANSFERRING DATA 0 TO N
NOTIFY OF UNTRANSFERABLE STATE OF READ DATA
S108

FIG. 3

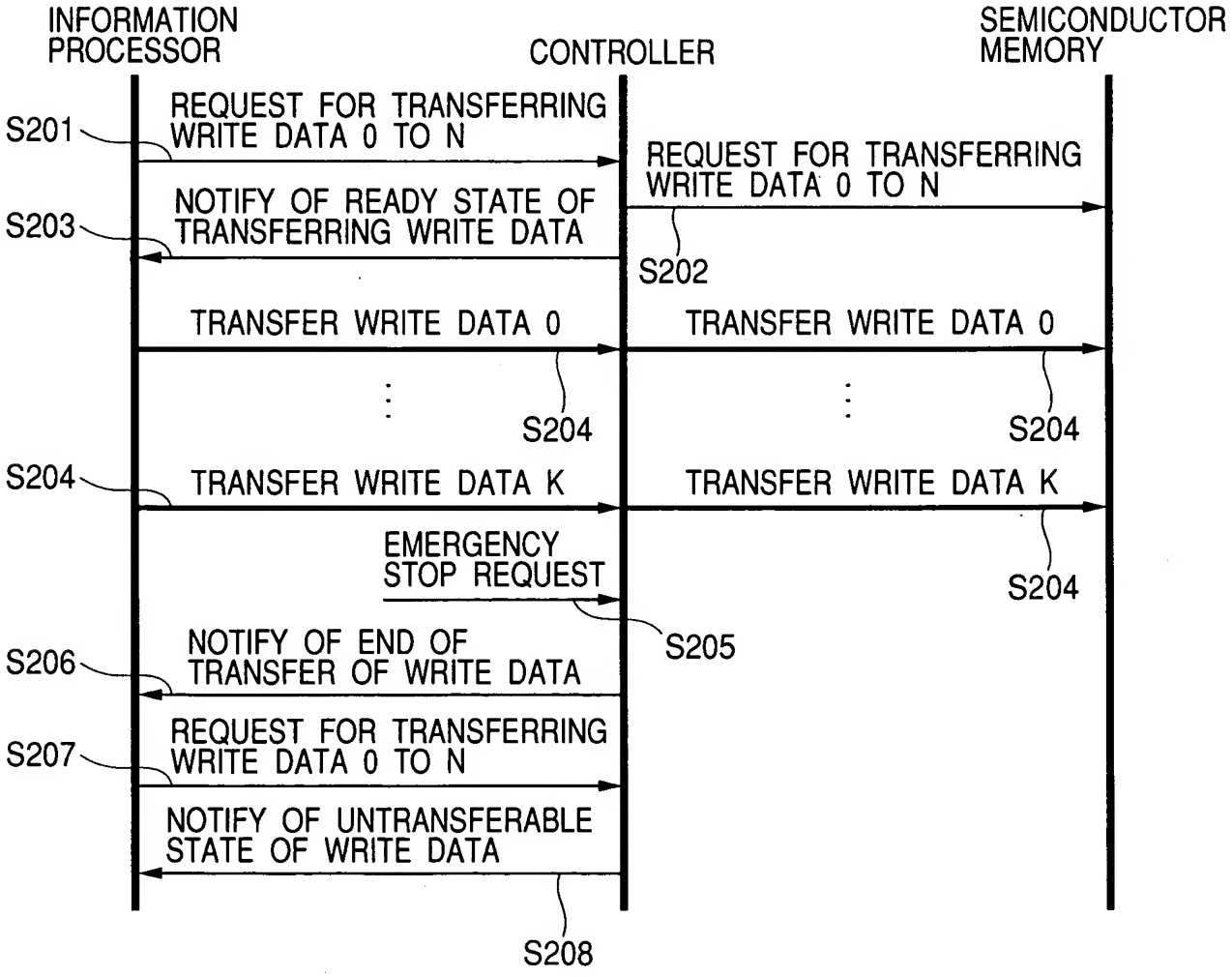

INFORMATION PROCESSOR
CONTROLLER
SEMICONDUCTOR MEMORY
S201
REQUEST FOR TRANSFERRING WRITE DATA 0 TO N
REQUEST FOR TRANSFERRING WRITE DATA 0 TO N
S203
NOTIFY OF READY STATE OF TRANSFERRING WRITE DATA
S202
TRANSFER WRITE DATA 0
TRANSFER WRITE DATA 0
S204
S204
S204
TRANSFER WRITE DATA K
TRANSFER WRITE DATA K
S204
EMERGENCY STOP REQUEST
S205
S206
NOTIFY OF END OF TRANSFER OF WRITE DATA
S207
REQUEST FOR TRANSFERRING WRITE DATA 0 TO N
NOTIFY OF UNTRANSFERABLE STATE OF WRITE DATA
S208

FIG. 4

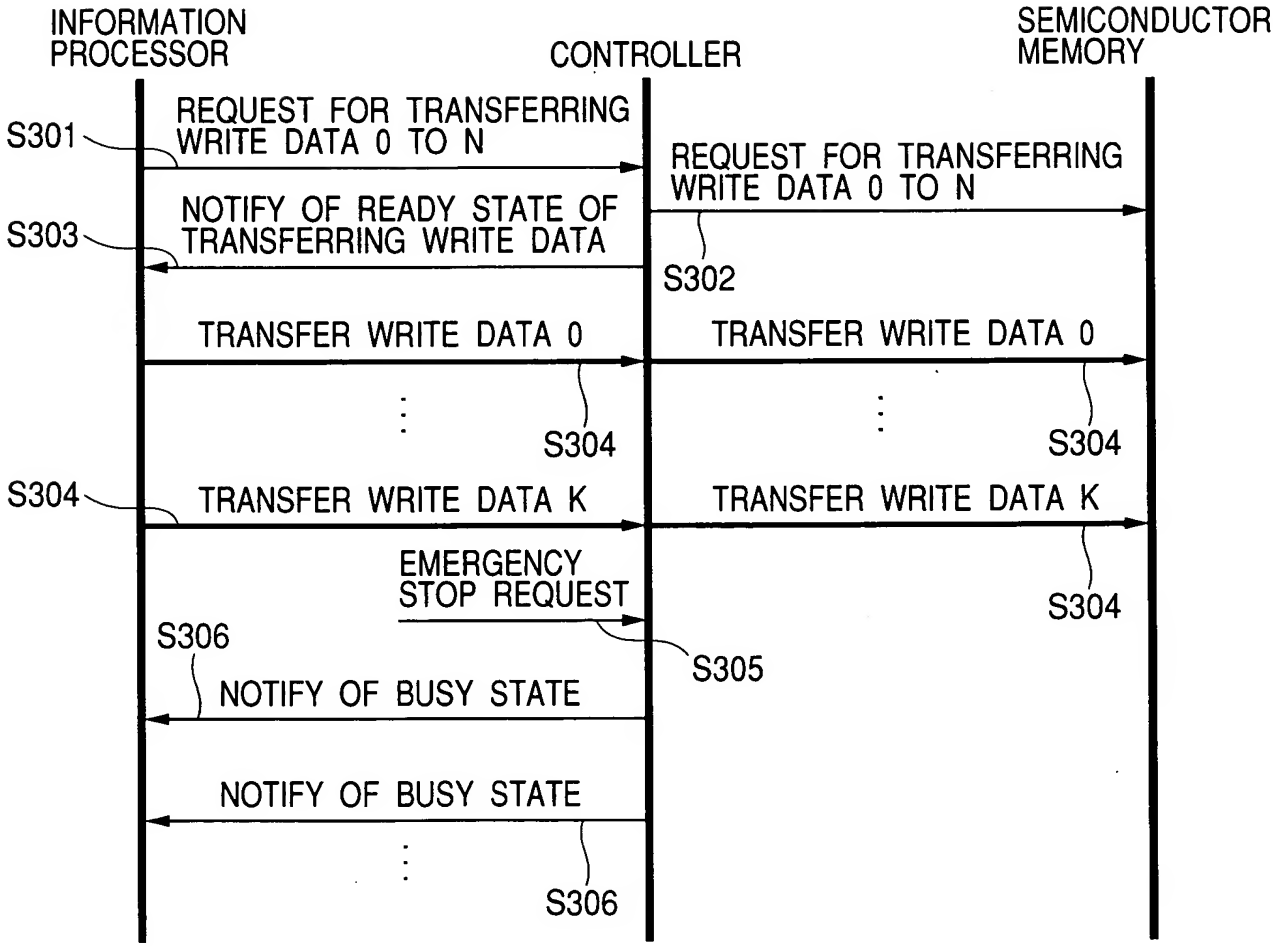

INFORMATION PROCESSOR
CONTROLLER
SEMICONDUCTOR MEMORY
S301
REQUEST FOR TRANSFERRING WRITE DATA 0 TO N
REQUEST FOR TRANSFERRING WRITE DATA 0 TO N
S303
NOTIFY OF READY STATE OF TRANSFERRING WRITE DATA
S302
TRANSFER WRITE DATA 0
TRANSFER WRITE DATA 0
S304
S304
S304
TRANSFER WRITE DATA K
TRANSFER WRITE DATA K
EMERGENCY STOP REQUEST
S304
S306
S305
NOTIFY OF BUSY STATE
NOTIFY OF BUSY STATE
S306

FIG. 5

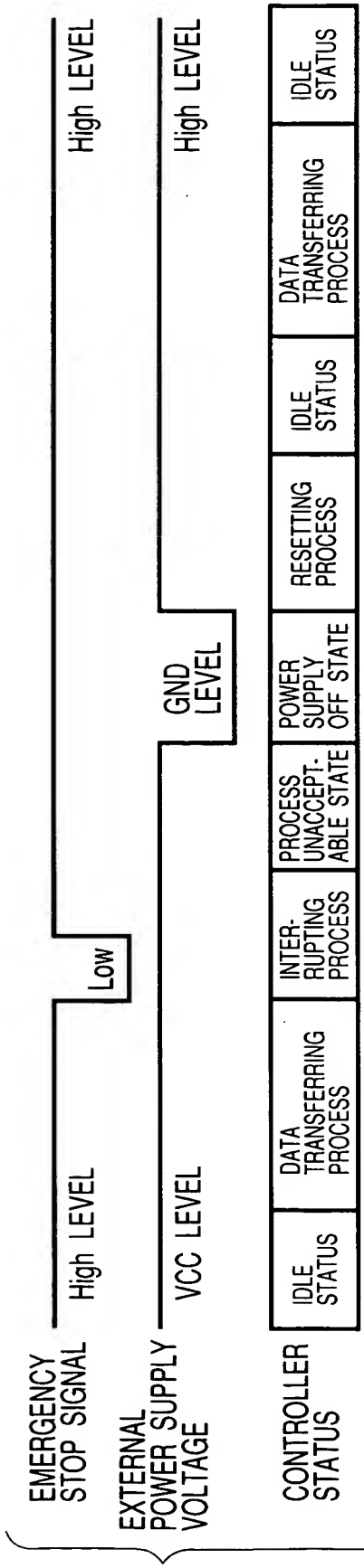

EMERGENCY STOP SIGNAL
High LEVEL
Low
High LEVEL
EXTERNAL POWER SUPPLY VOLTAGE
VCC LEVEL
GND LEVEL
CONTROLLER STATUS
IDLE STATUS
DATA TRANSFERRING PROCESS
INTER-RUPTING PROCESS
PROCESS UNACCEPT-ABLE STATE
POWER SUPPLY OFF STATE
RESETTING PROCESS
IDLE STATUS
DATA TRANSFERRING PROCESS
IDLE STATUS

FIG. 6

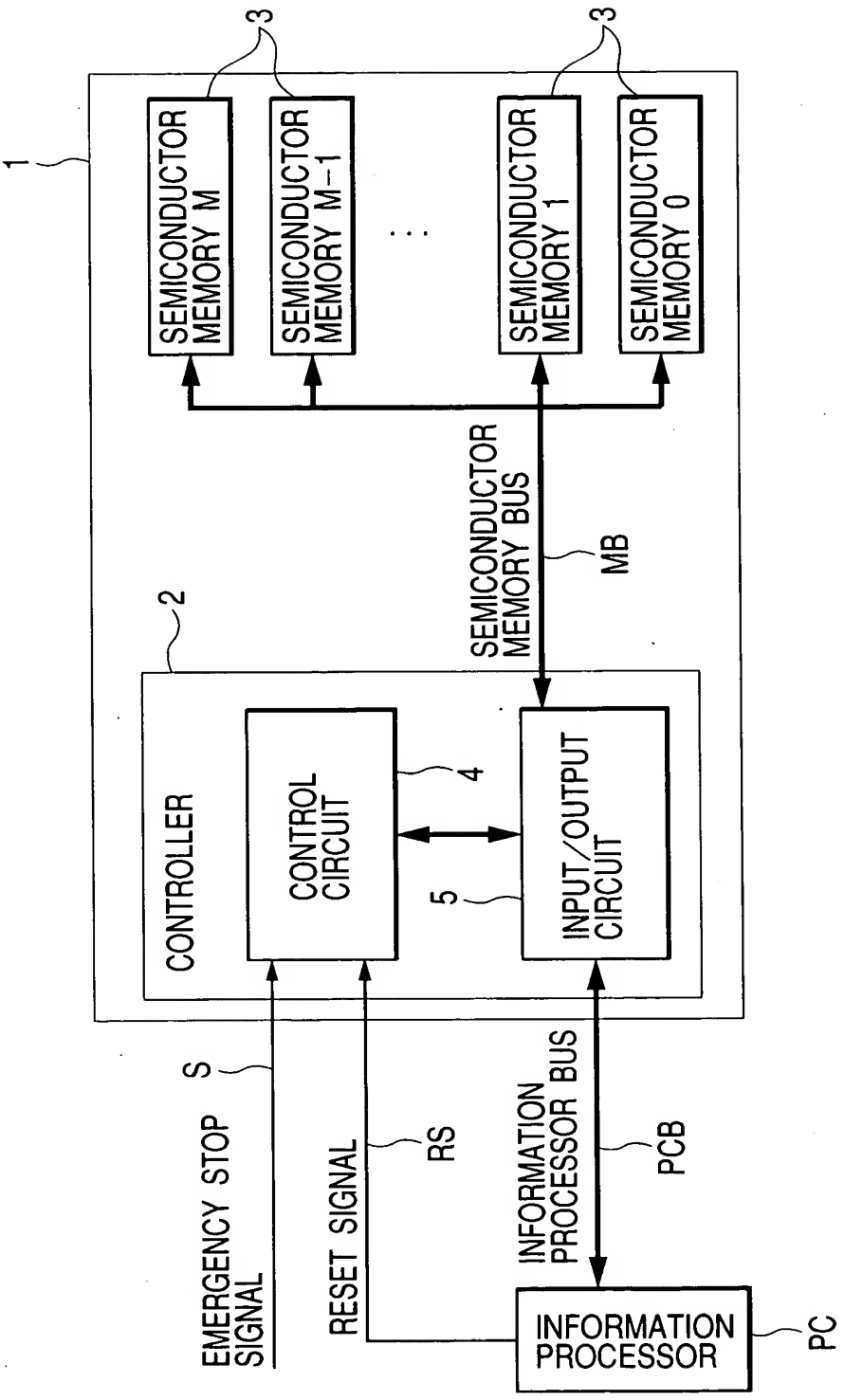

1
3
3
SEMICONDUCTOR MEMORY M
SEMICONDUCTOR MEMORY M−1
SEMICONDUCTOR MEMORY 1
SEMICONDUCTOR MEMORY 0
SEMICONDUCTOR MEMORY BUS
MB
2
CONTROLLER
CONTROL CIRCUIT
4
5
INPUT/OUTPUT CIRCUIT
S
EMERGENCY STOP SIGNAL
RESET SIGNAL
RS
INFORMATION PROCESSOR BUS
PCB
INFORMATION PROCESSOR
PC

FIG. 7

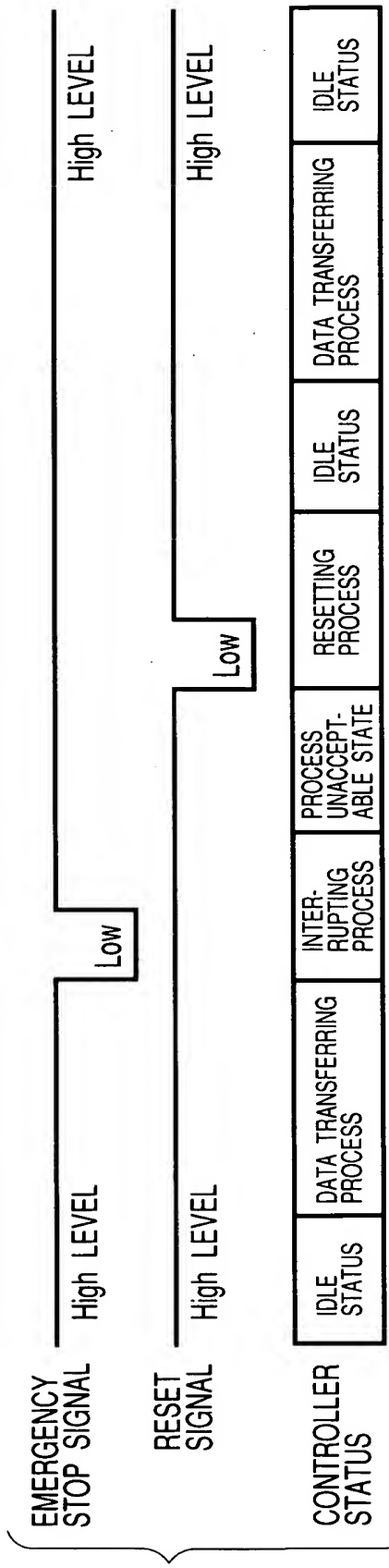

EMERGENCY STOP SIGNAL
High LEVEL
Low
High LEVEL
RESET SIGNAL
High LEVEL
Low
High LEVEL
CONTROLLER STATUS
IDLE STATUS
DATA TRANSFERRING PROCESS
INTER-RUPTING PROCESS
PROCESS UNACCEPT-ABLE STATE
RESETTING PROCESS
IDLE STATUS
DATA TRANSFERRING PROCESS
IDLE STATUS

FIG. 8

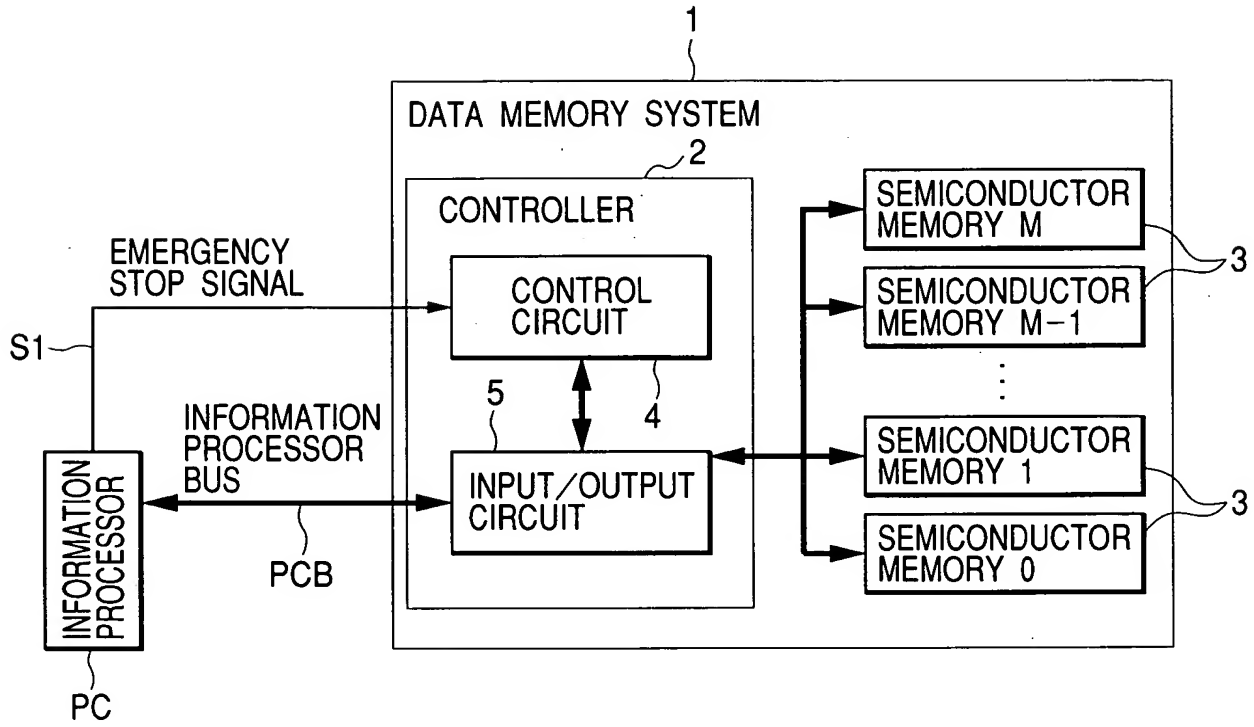

1
DATA MEMORY SYSTEM
2
CONTROLLER
CONTROL CIRCUIT
INPUT/OUTPUT CIRCUIT
5
4
EMERGENCY STOP SIGNAL
S1
INFORMATION PROCESSOR BUS
PCB
INFORMATION PROCESSOR
PC
SEMICONDUCTOR MEMORY M
SEMICONDUCTOR MEMORY M−1
SEMICONDUCTOR MEMORY 1
SEMICONDUCTOR MEMORY 0
3
3

FIG. 9

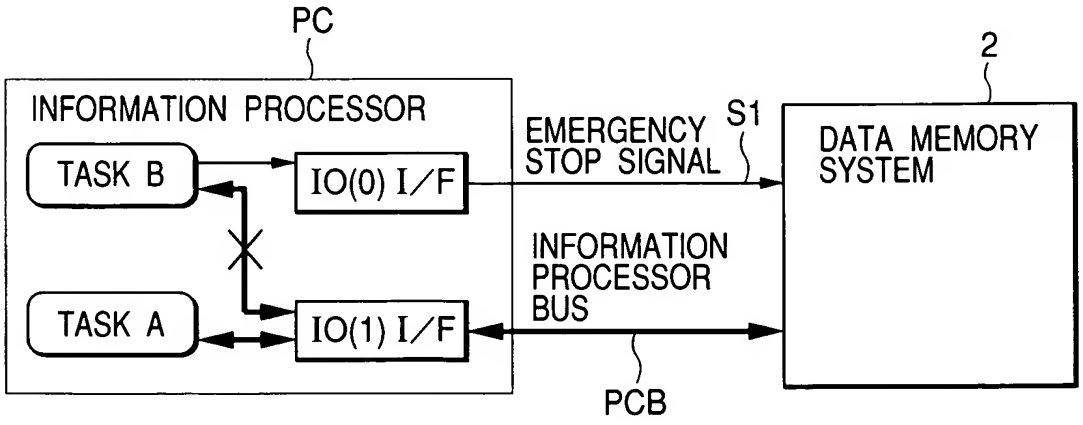

PC
INFORMATION PROCESSOR
TASK B
TASK A
IO(0) I/F
IO(1) I/F
EMERGENCY STOP SIGNAL
S1
INFORMATION PROCESSOR BUS
PCB
2
DATA MEMORY SYSTEM

FIG. 10

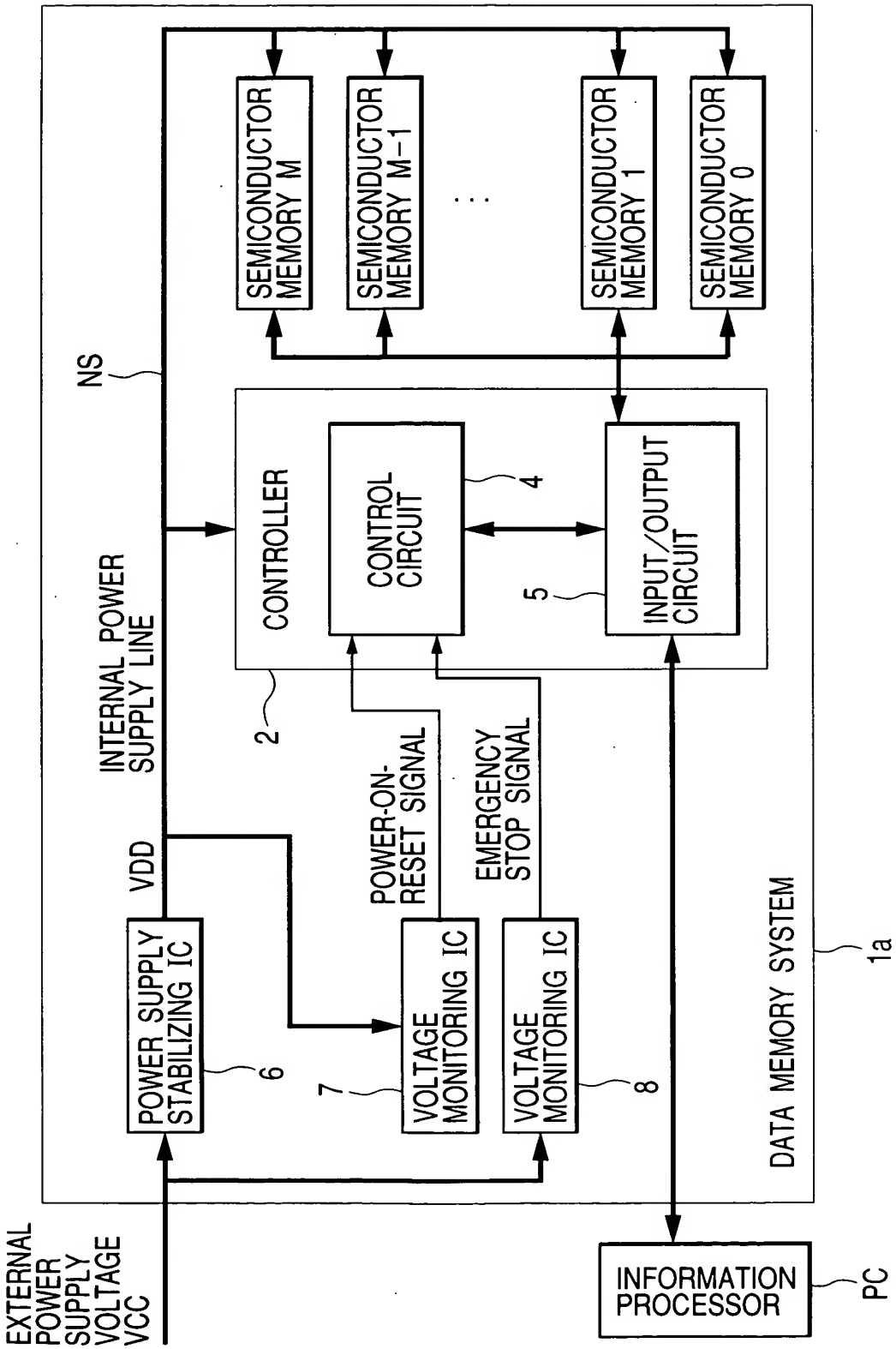

SEMICONDUCTOR MEMORY M
SEMICONDUCTOR MEMORY M−1
SEMICONDUCTOR MEMORY 1
SEMICONDUCTOR MEMORY 0
NS
CONTROLLER
CONTROL CIRCUIT
4
INPUT/OUTPUT CIRCUIT
5
2
INTERNAL POWER SUPPLY LINE
VDD
POWER-ON-RESET SIGNAL
EMERGENCY STOP SIGNAL
POWER SUPPLY STABILIZING IC
6
VOLTAGE MONITORING IC
7
VOLTAGE MONITORING IC
8
DATA MEMORY SYSTEM
1a
EXTERNAL POWER SUPPLY VOLTAGE VCC
INFORMATION PROCESSOR
PC

FIG. 11

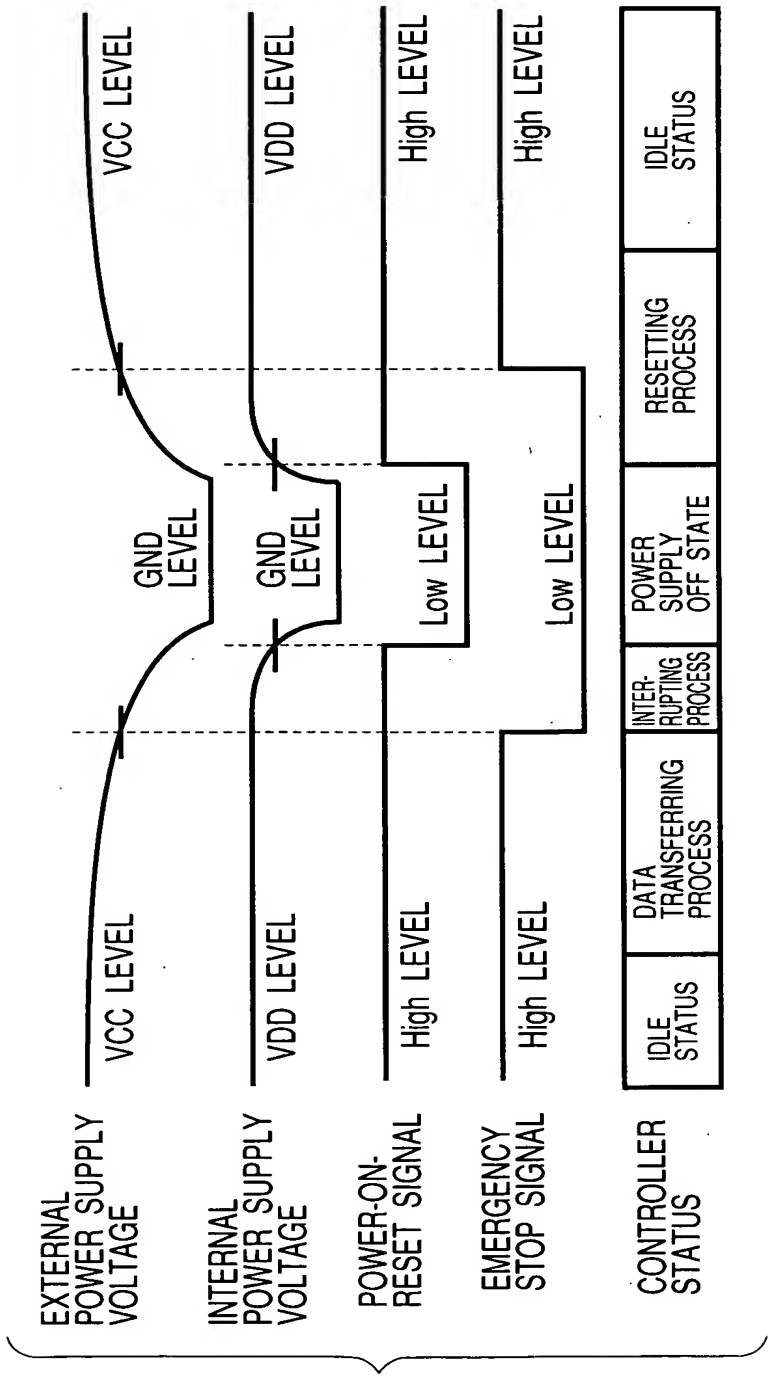

EXTERNAL POWER SUPPLY VOLTAGE
VCC LEVEL
GND LEVEL
VCC LEVEL
INTERNAL POWER SUPPLY VOLTAGE
VDD LEVEL
GND LEVEL
VDD LEVEL
POWER-ON-RESET SIGNAL
High LEVEL
Low LEVEL
High LEVEL
EMERGENCY STOP SIGNAL
High LEVEL
Low LEVEL
High LEVEL
CONTROLLER STATUS
IDLE STATUS
DATA TRANSFERRING PROCESS
INTER-RUPTING PROCESS
POWER SUPPLY OFF STATE
RESETTING PROCESS
IDLE STATUS

FIG. 12

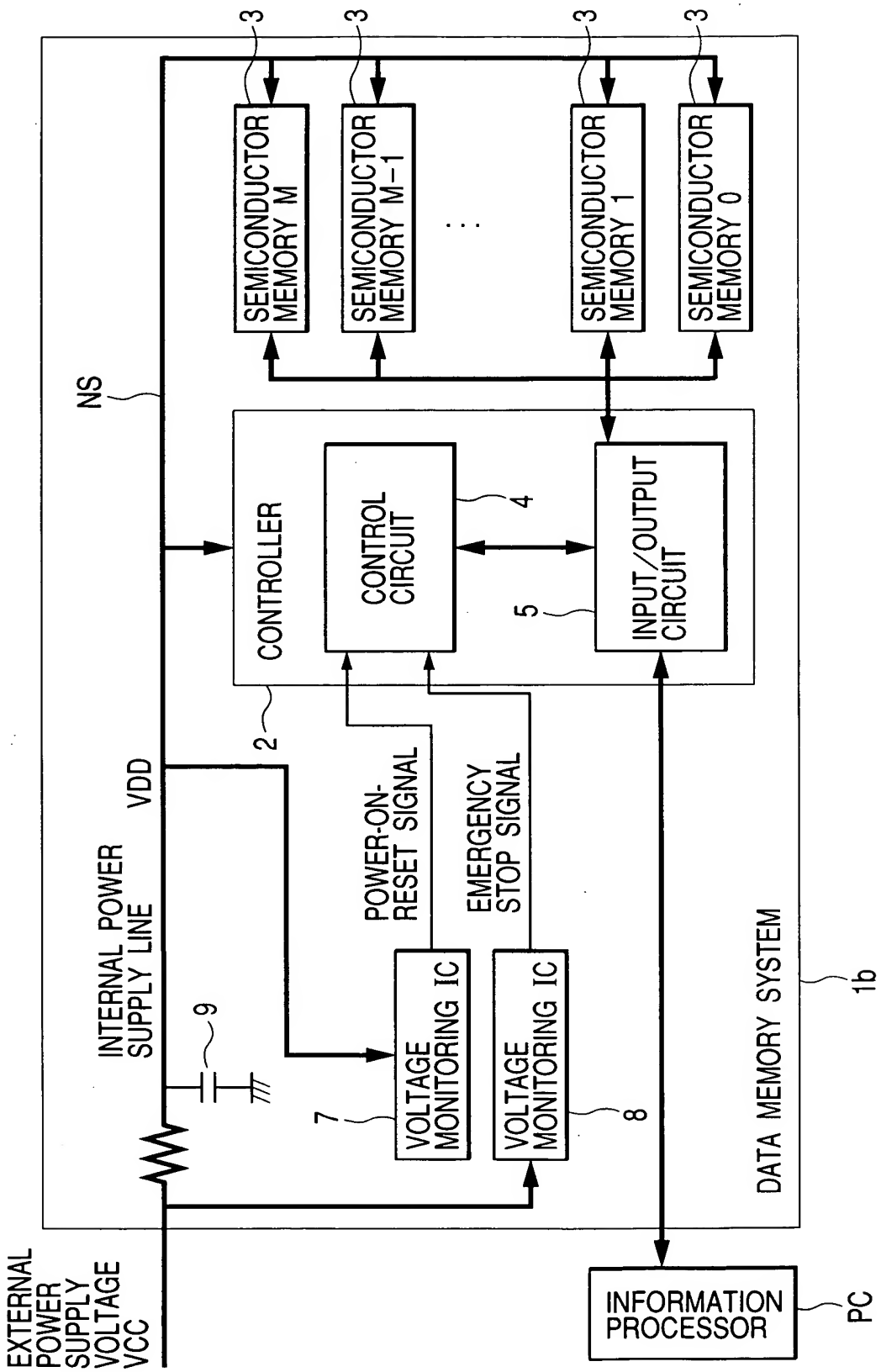

SEMICONDUCTOR MEMORY M
SEMICONDUCTOR MEMORY M-1
SEMICONDUCTOR MEMORY 1
SEMICONDUCTOR MEMORY 0
3
NS
CONTROLLER
CONTROL CIRCUIT
INPUT/OUTPUT CIRCUIT
4
5
2
VDD
INTERNAL POWER SUPPLY LINE
POWER-ON-RESET SIGNAL
EMERGENCY STOP SIGNAL
9
7
8
VOLTAGE MONITORING IC
VOLTAGE MONITORING IC
DATA MEMORY SYSTEM
1b
EXTERNAL POWER SUPPLY VOLTAGE VCC
INFORMATION PROCESSOR
PC

FIG. 13

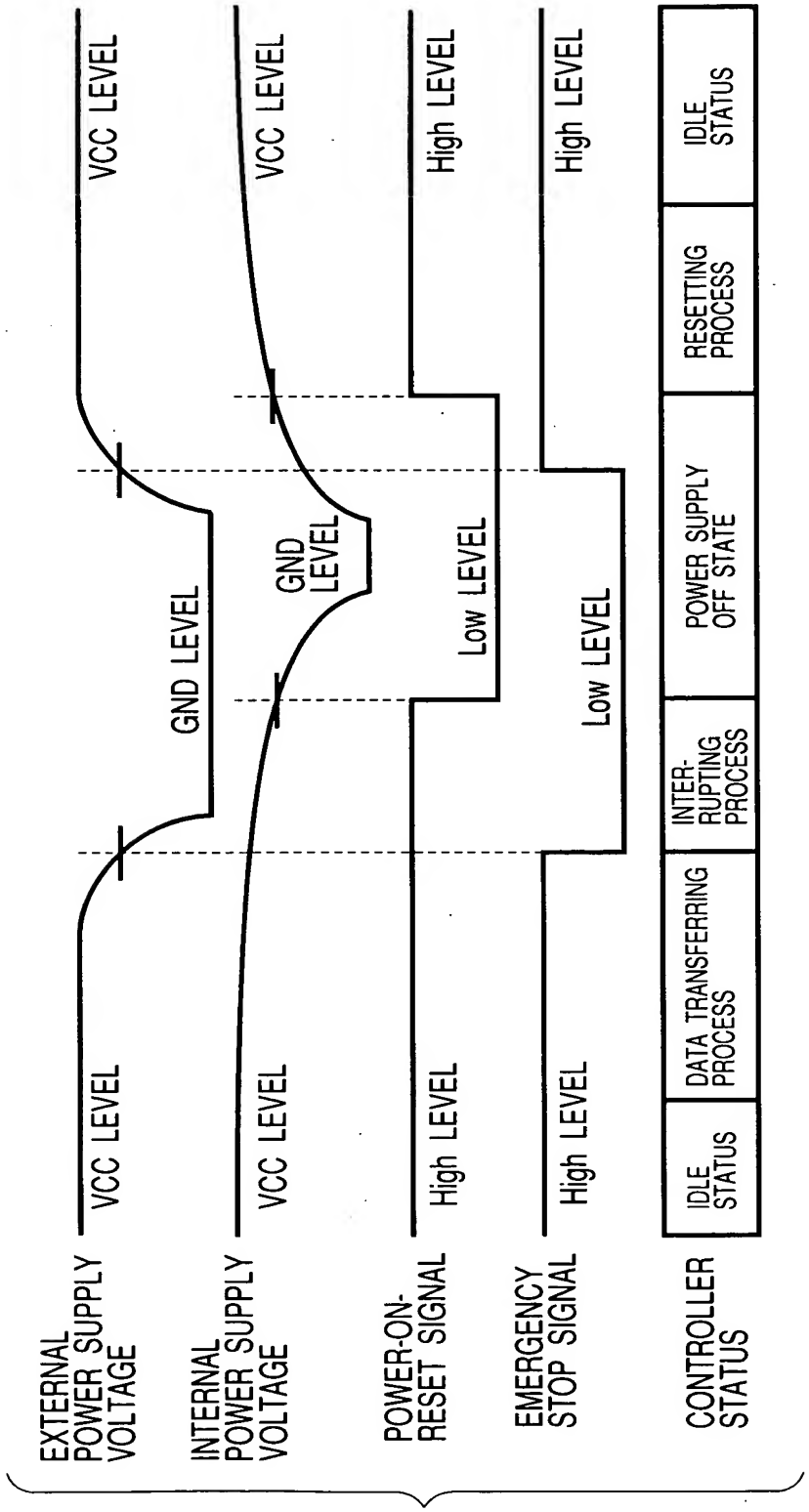

EXTERNAL POWER SUPPLY VOLTAGE
VCC LEVEL
GND LEVEL
VCC LEVEL
INTERNAL POWER SUPPLY VOLTAGE
GND LEVEL
VCC LEVEL
POWER-ON-RESET SIGNAL
High LEVEL
Low LEVEL
High LEVEL
EMERGENCY STOP SIGNAL
High LEVEL
Low LEVEL
High LEVEL
CONTROLLER STATUS
IDLE STATUS
DATA TRANSFERRING PROCESS
INTER-RUPTING PROCESS
POWER SUPPLY OFF STATE
RESETTING PROCESS
IDLE STATUS

FIG. 14

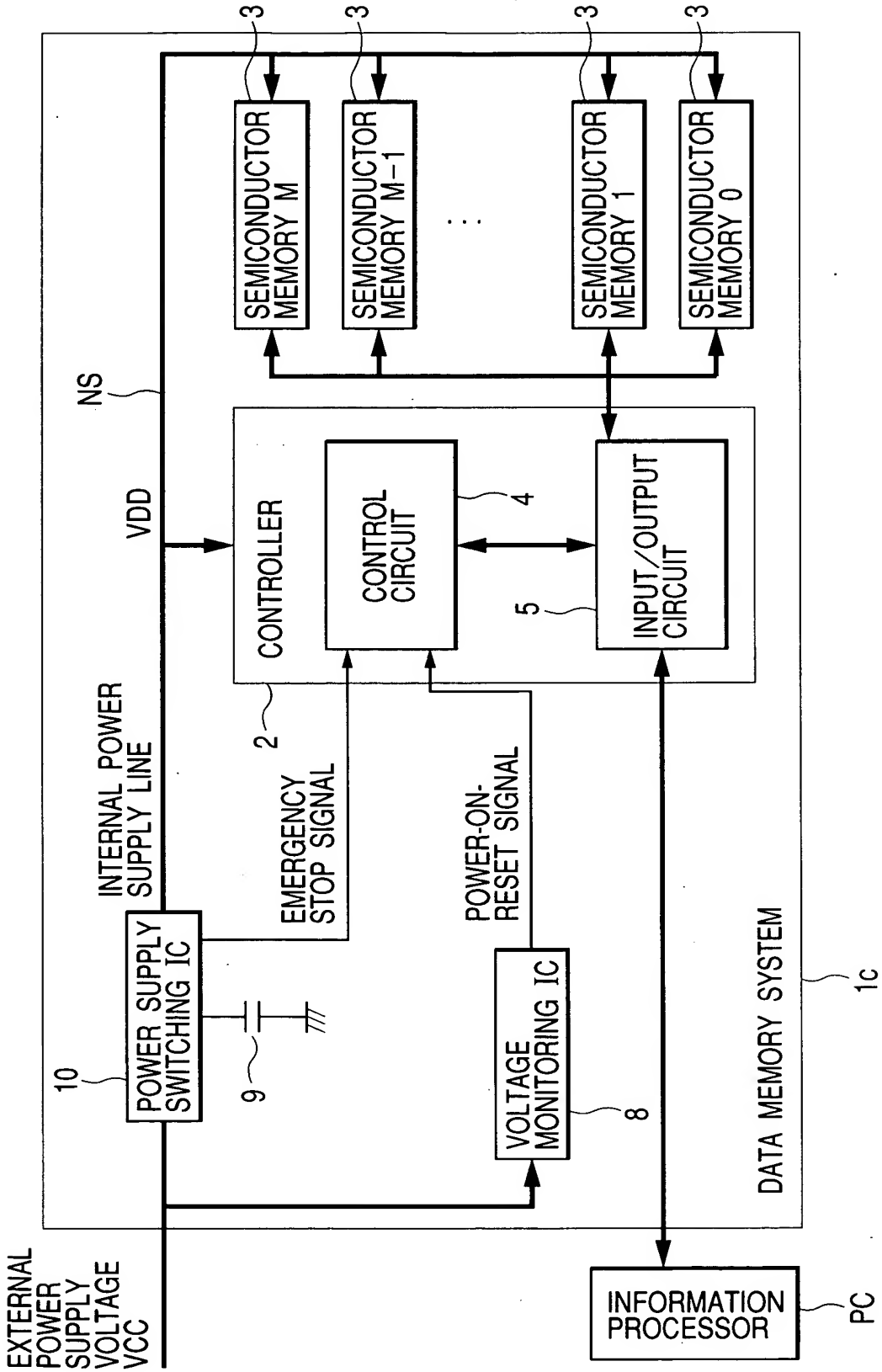

EXTERNAL POWER SUPPLY VOLTAGE VCC
DATA MEMORY SYSTEM
1c
INFORMATION PROCESSOR
PC
POWER SUPPLY SWITCHING IC
10
9
VOLTAGE MONITORING IC
8
INTERNAL POWER SUPPLY LINE
EMERGENCY STOP SIGNAL
POWER-ON-RESET SIGNAL
NS
VDD
CONTROLLER
2
CONTROL CIRCUIT
4
INPUT/OUTPUT CIRCUIT
5
SEMICONDUCTOR MEMORY M
SEMICONDUCTOR MEMORY M-1
SEMICONDUCTOR MEMORY 1
SEMICONDUCTOR MEMORY 0
3

FIG. 15

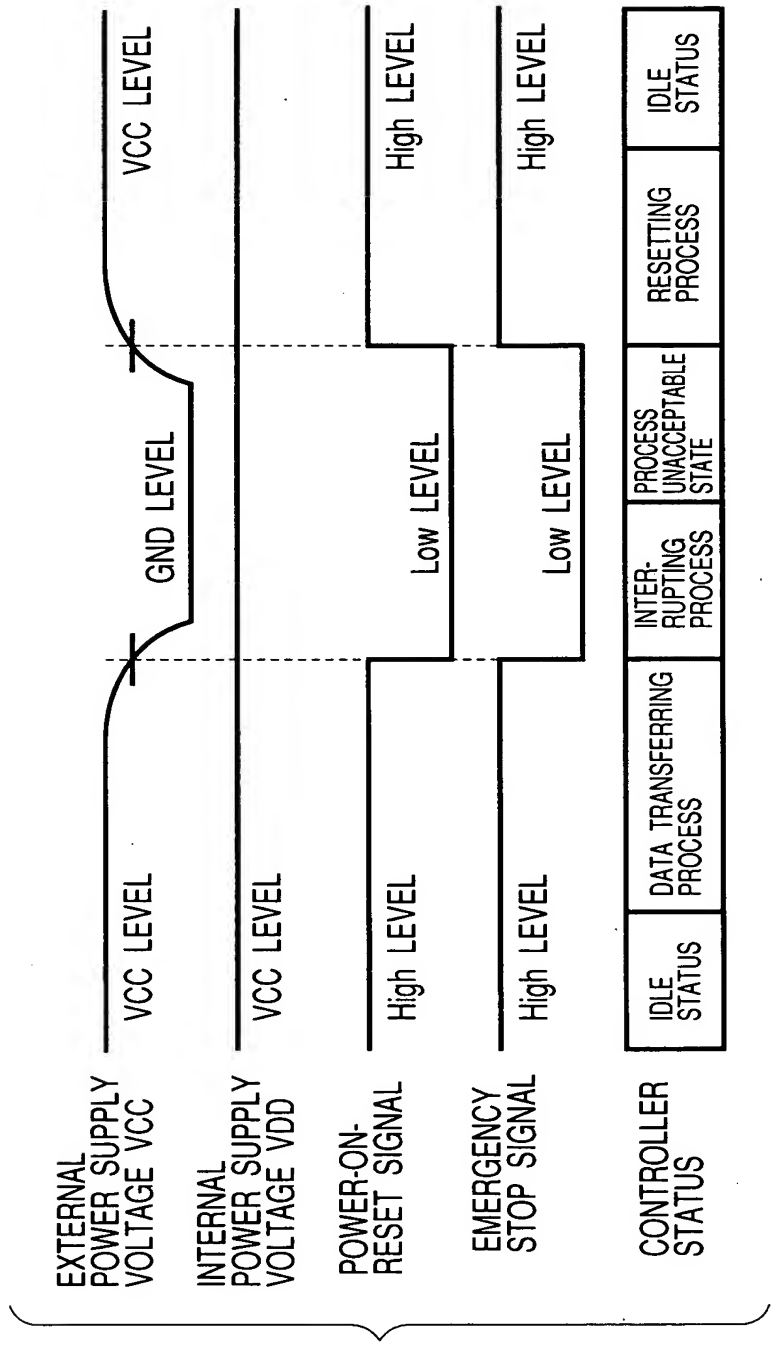

EXTERNAL POWER SUPPLY VOLTAGE VCC
INTERNAL POWER SUPPLY VOLTAGE VDD
POWER-ON-RESET SIGNAL
EMERGENCY STOP SIGNAL
CONTROLLER STATUS
VCC LEVEL
GND LEVEL
VCC LEVEL
VCC LEVEL
High LEVEL
Low LEVEL
High LEVEL
High LEVEL
Low LEVEL
High LEVEL
IDLE STATUS
DATA TRANSFERRING PROCESS
INTER-RUPTING PROCESS
PROCESS UNACCEPTABLE STATE
RESETTING PROCESS
IDLE STATUS

FIG. 16

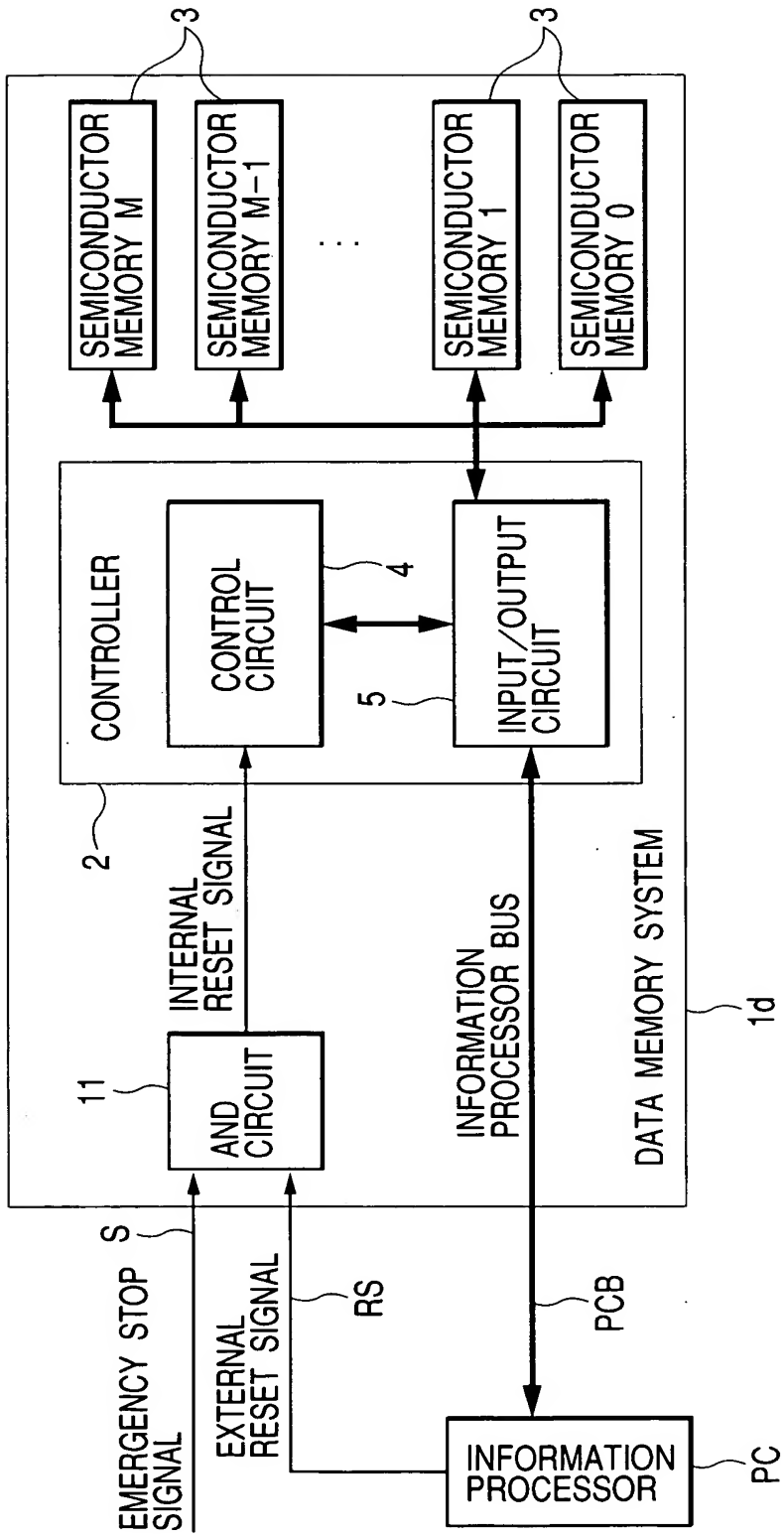

3
3
SEMICONDUCTOR MEMORY M
SEMICONDUCTOR MEMORY M-1
SEMICONDUCTOR MEMORY 1
SEMICONDUCTOR MEMORY 0
CONTROLLER
CONTROL CIRCUIT
4
5
INPUT/OUTPUT CIRCUIT
2
INTERNAL RESET SIGNAL
11
AND CIRCUIT
INFORMATION PROCESSOR BUS
DATA MEMORY SYSTEM
1d
S
EMERGENCY STOP SIGNAL
EXTERNAL RESET SIGNAL
RS
PCB
INFORMATION PROCESSOR
PC

FIG. 17

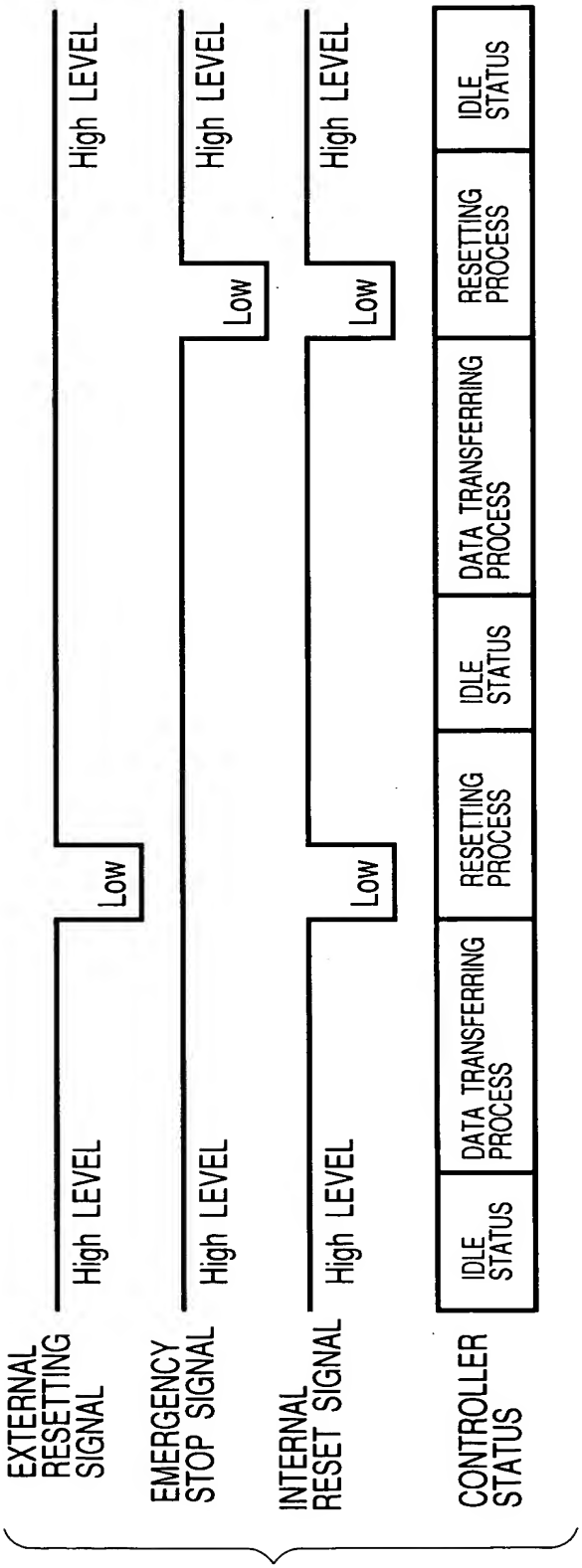

EXTERNAL RESETTING SIGNAL
High LEVEL
Low
High LEVEL
EMERGENCY STOP SIGNAL
High LEVEL
Low
High LEVEL
INTERNAL RESET SIGNAL
High LEVEL
Low
High LEVEL
CONTROLLER STATUS
IDLE STATUS
DATA TRANSFERRING PROCESS
RESETTING PROCESS
IDLE STATUS
DATA TRANSFERRING PROCESS
RESETTING PROCESS
IDLE STATUS

FIG. 18

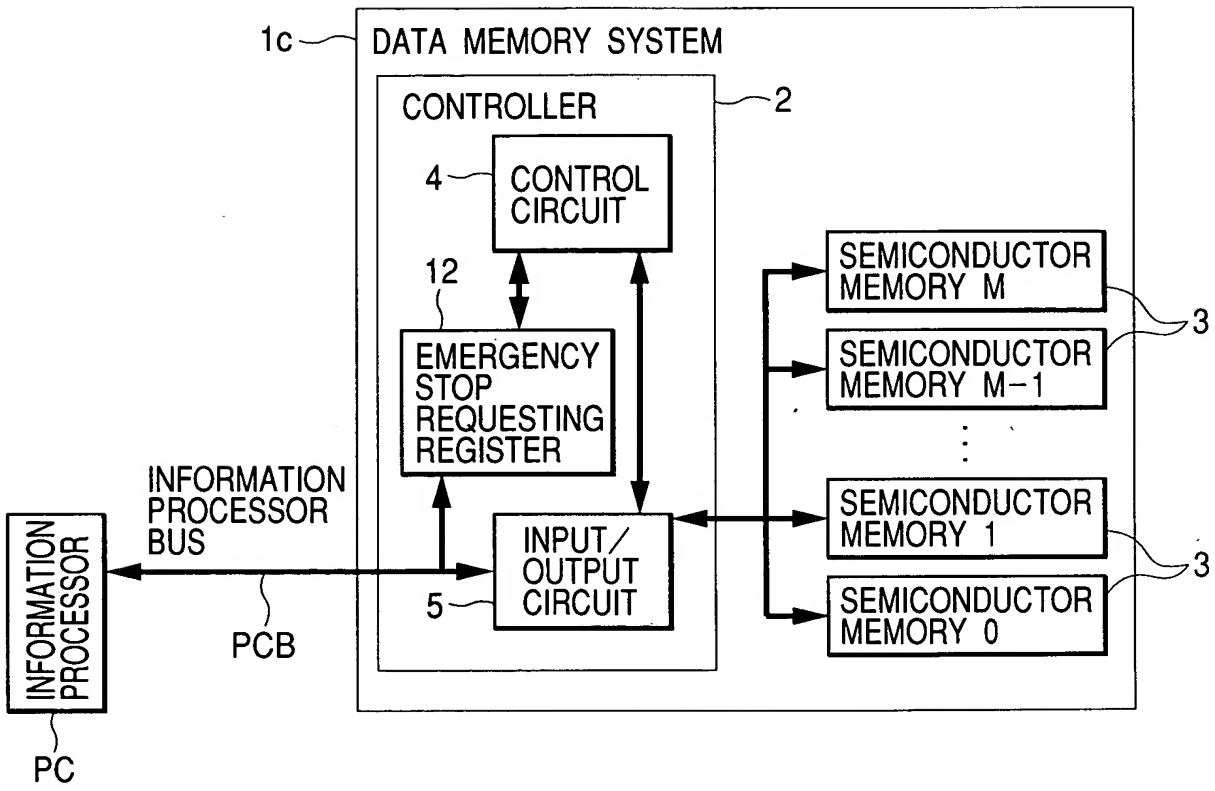


FIG. 19

EMERGENCY STOP REQUESTING REGISTER
STATUS REGISTER
ADDRESS REGISTER
PROCESS REQUESTING REGISTER
DATA INPUT/OUTPUT REGISTER

FIG. 20

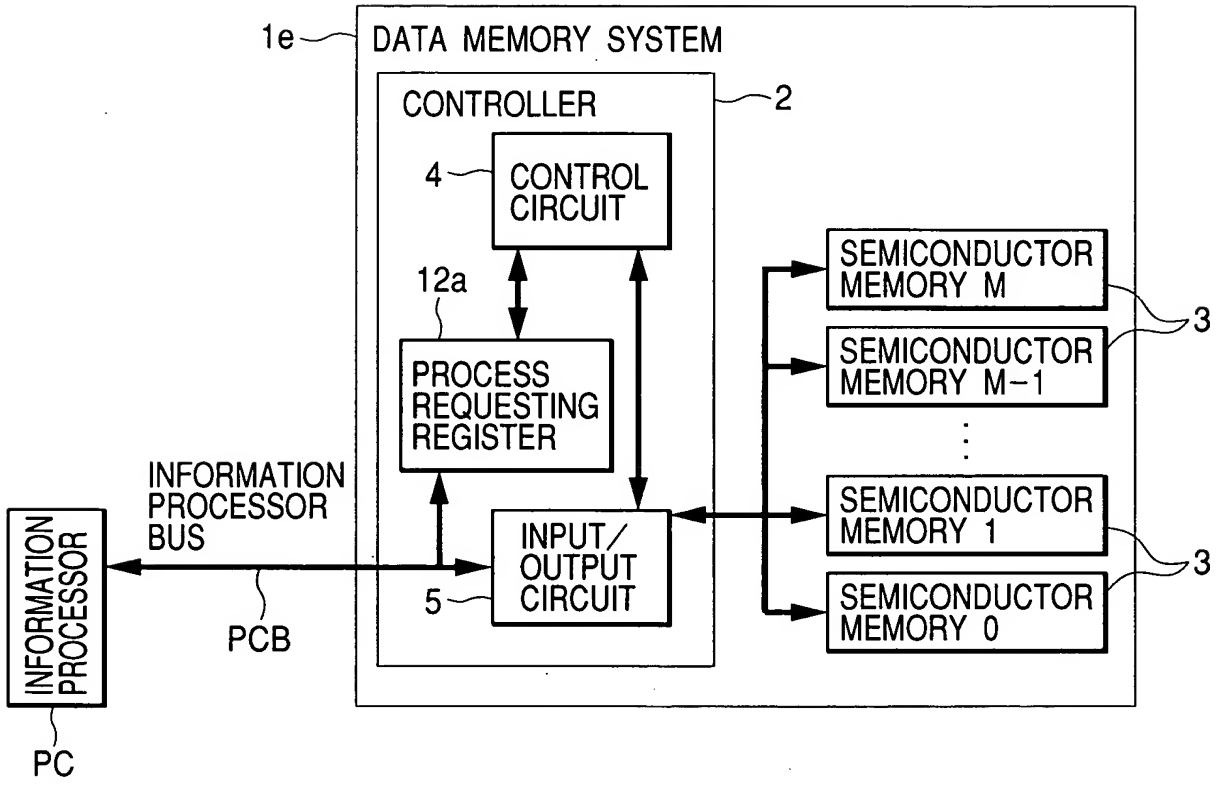
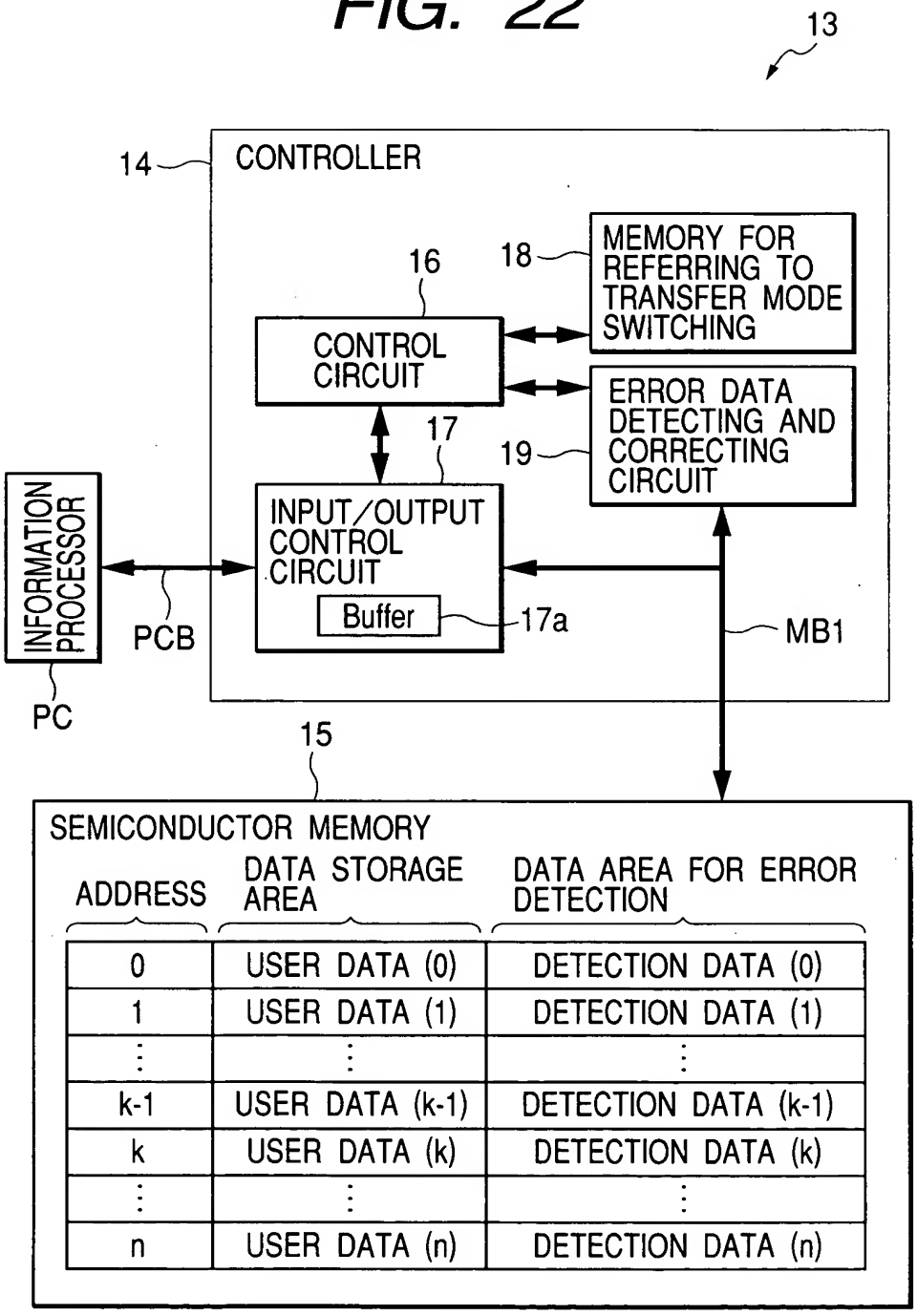


FIG. 21

STATUS REGISTER
ADDRESS REGISTER
PROCESS REQUESTING REGISTER
DATA INPUT/OUTPUT REGISTER

FIG. 22



ADDRESS	DATA STORAGE AREA	DATA AREA FOR ERROR DETECTION
0	USER DATA (0)	DETECTION DATA (0)
1	USER DATA (1)	DETECTION DATA (1)
⋮	⋮	⋮
k-1	USER DATA (k-1)	DETECTION DATA (k-1)
k	USER DATA (k)	DETECTION DATA (k)
⋮	⋮	⋮
n	USER DATA (n)	DETECTION DATA (n)

FIG. 23

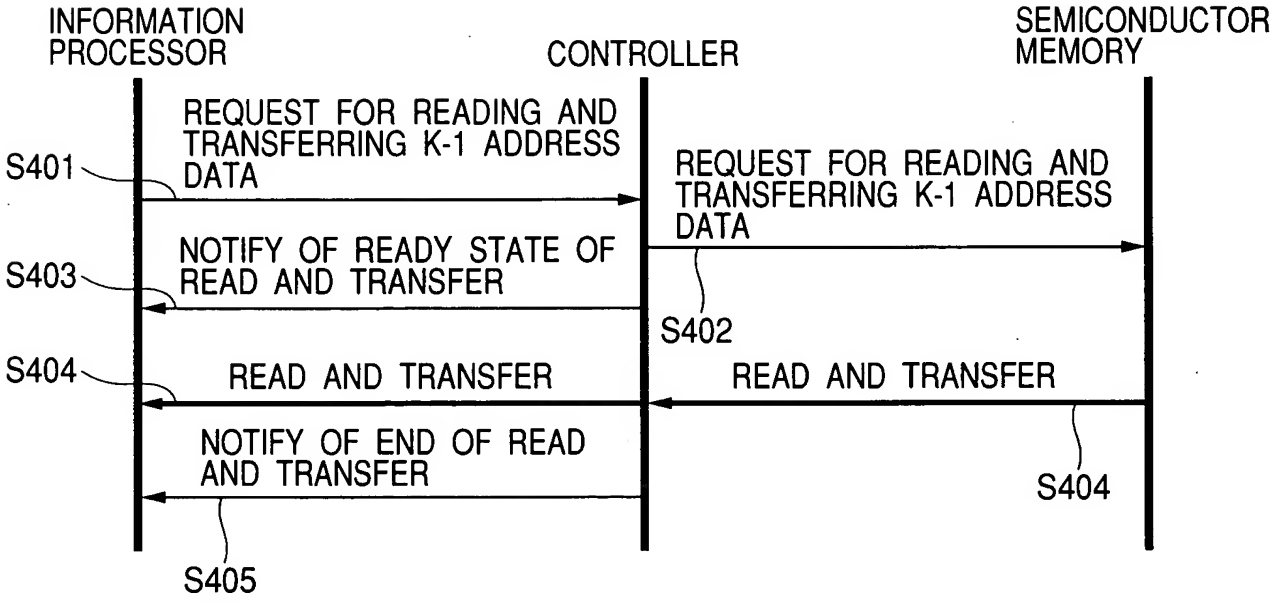

INFORMATION PROCESSOR
CONTROLLER
SEMICONDUCTOR MEMORY
S401
REQUEST FOR READING AND TRANSFERRING K-1 ADDRESS DATA
REQUEST FOR READING AND TRANSFERRING K-1 ADDRESS DATA
S403
NOTIFY OF READY STATE OF READ AND TRANSFER
S402
S404
READ AND TRANSFER
READ AND TRANSFER
NOTIFY OF END OF READ AND TRANSFER
S404
S405

FIG. 24

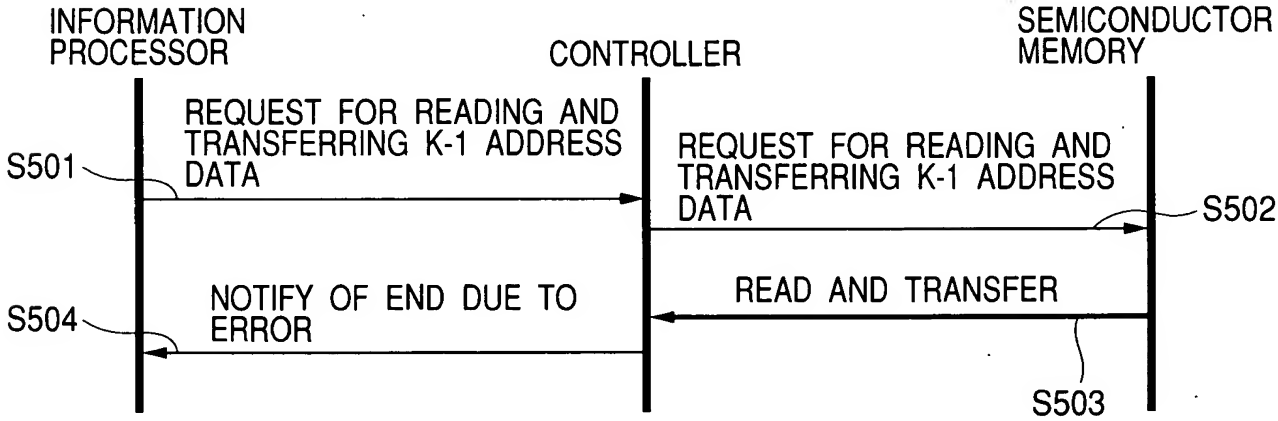

INFORMATION PROCESSOR
CONTROLLER
SEMICONDUCTOR MEMORY
S501
REQUEST FOR READING AND TRANSFERRING K-1 ADDRESS DATA
REQUEST FOR READING AND TRANSFERRING K-1 ADDRESS DATA
S502
S504
NOTIFY OF END DUE TO ERROR
READ AND TRANSFER
S503

FIG. 25

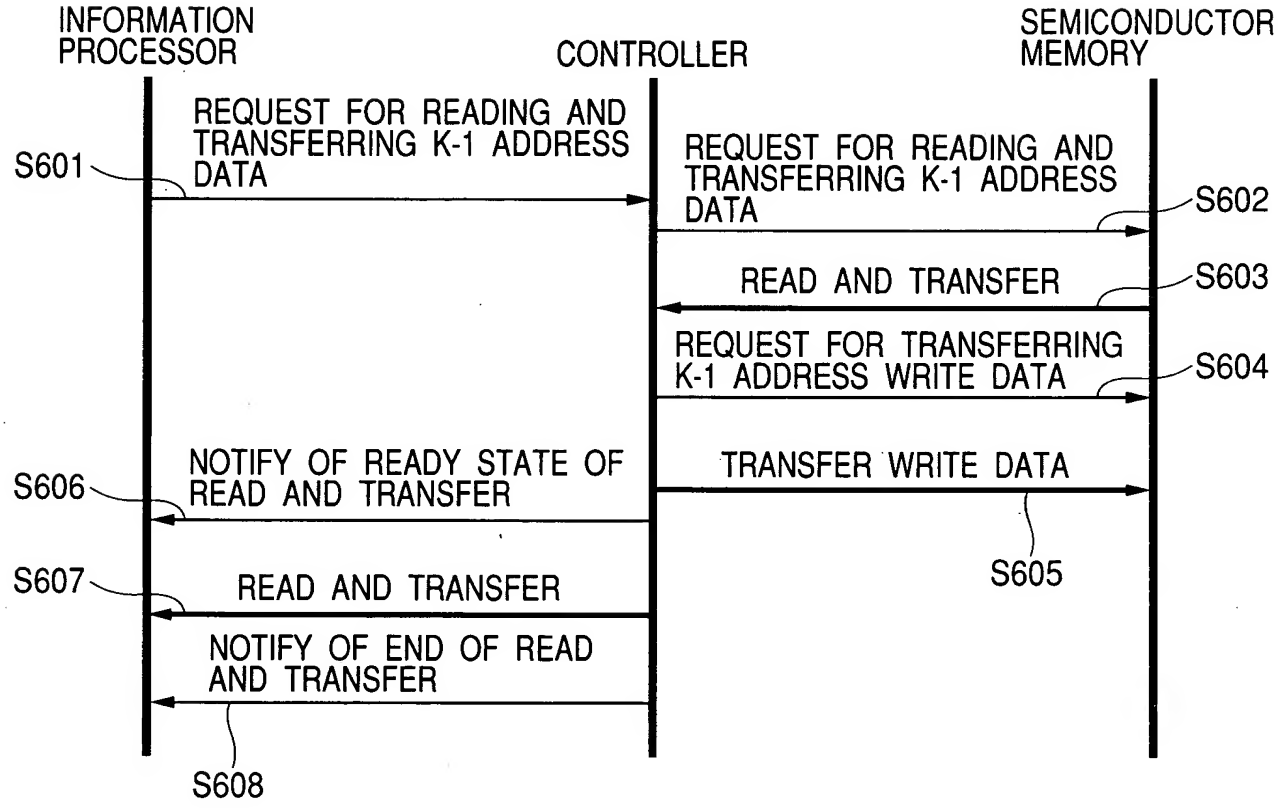

INFORMATION PROCESSOR
CONTROLLER
SEMICONDUCTOR MEMORY
S601
REQUEST FOR READING AND TRANSFERRING K-1 ADDRESS DATA
REQUEST FOR READING AND TRANSFERRING K-1 ADDRESS DATA
S602
READ AND TRANSFER
S603
REQUEST FOR TRANSFERRING K-1 ADDRESS WRITE DATA
S604
S606
NOTIFY OF READY STATE OF READ AND TRANSFER
TRANSFER WRITE DATA
S605
S607
READ AND TRANSFER
NOTIFY OF END OF READ AND TRANSFER
S608

FIG. 26

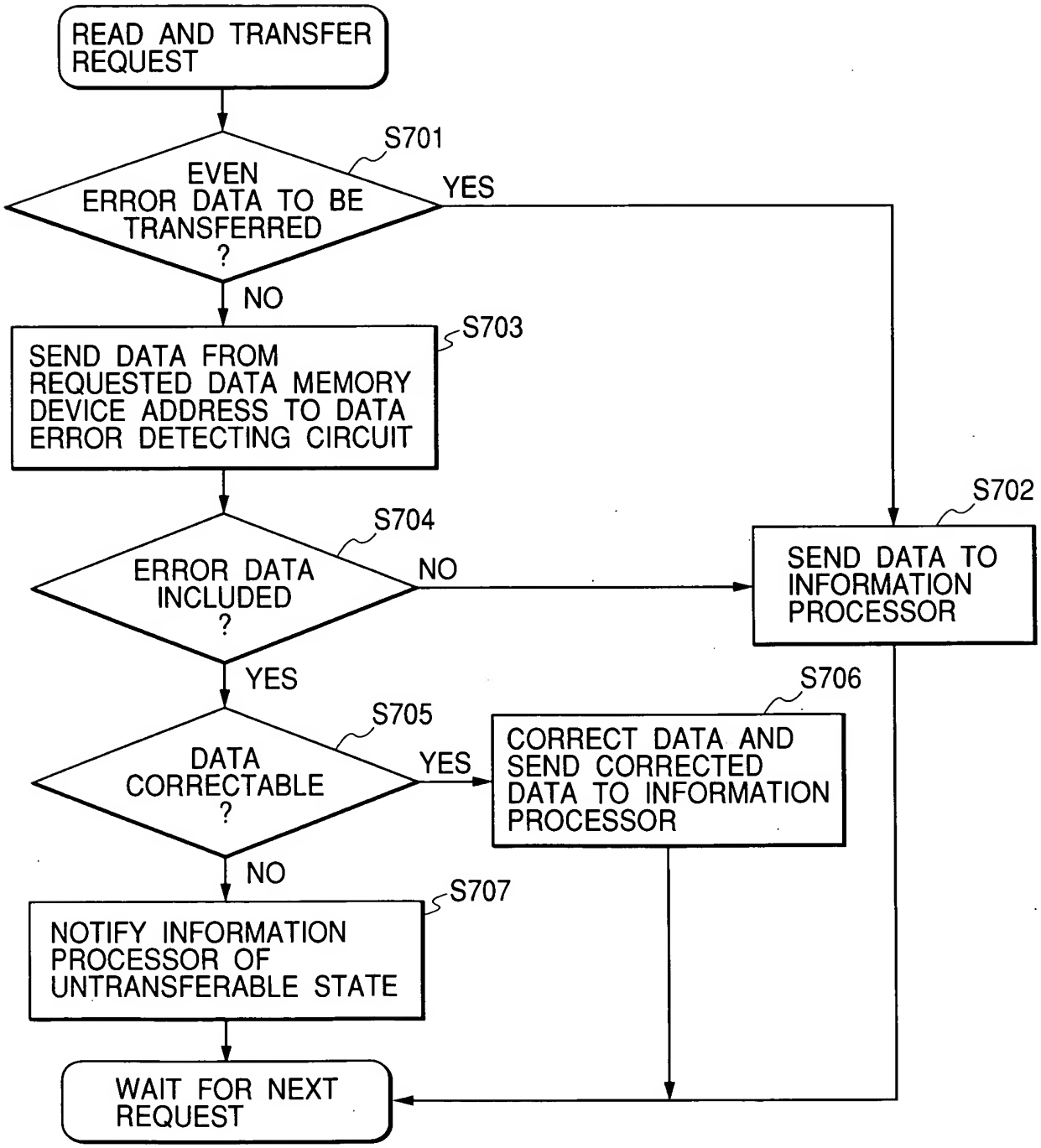

READ AND TRANSFER REQUEST
S701
EVEN ERROR DATA TO BE TRANSFERRED ?
YES
NO
S703
SEND DATA FROM REQUESTED DATA MEMORY DEVICE ADDRESS TO DATA ERROR DETECTING CIRCUIT
S704
ERROR DATA INCLUDED ?
NO
S702
SEND DATA TO INFORMATION PROCESSOR
YES
S705
DATA CORRECTABLE ?
YES
S706
CORRECT DATA AND SEND CORRECTED DATA TO INFORMATION PROCESSOR
NO
S707
NOTIFY INFORMATION PROCESSOR OF UNTRANSFERABLE STATE
WAIT FOR NEXT REQUEST

FIG. 27

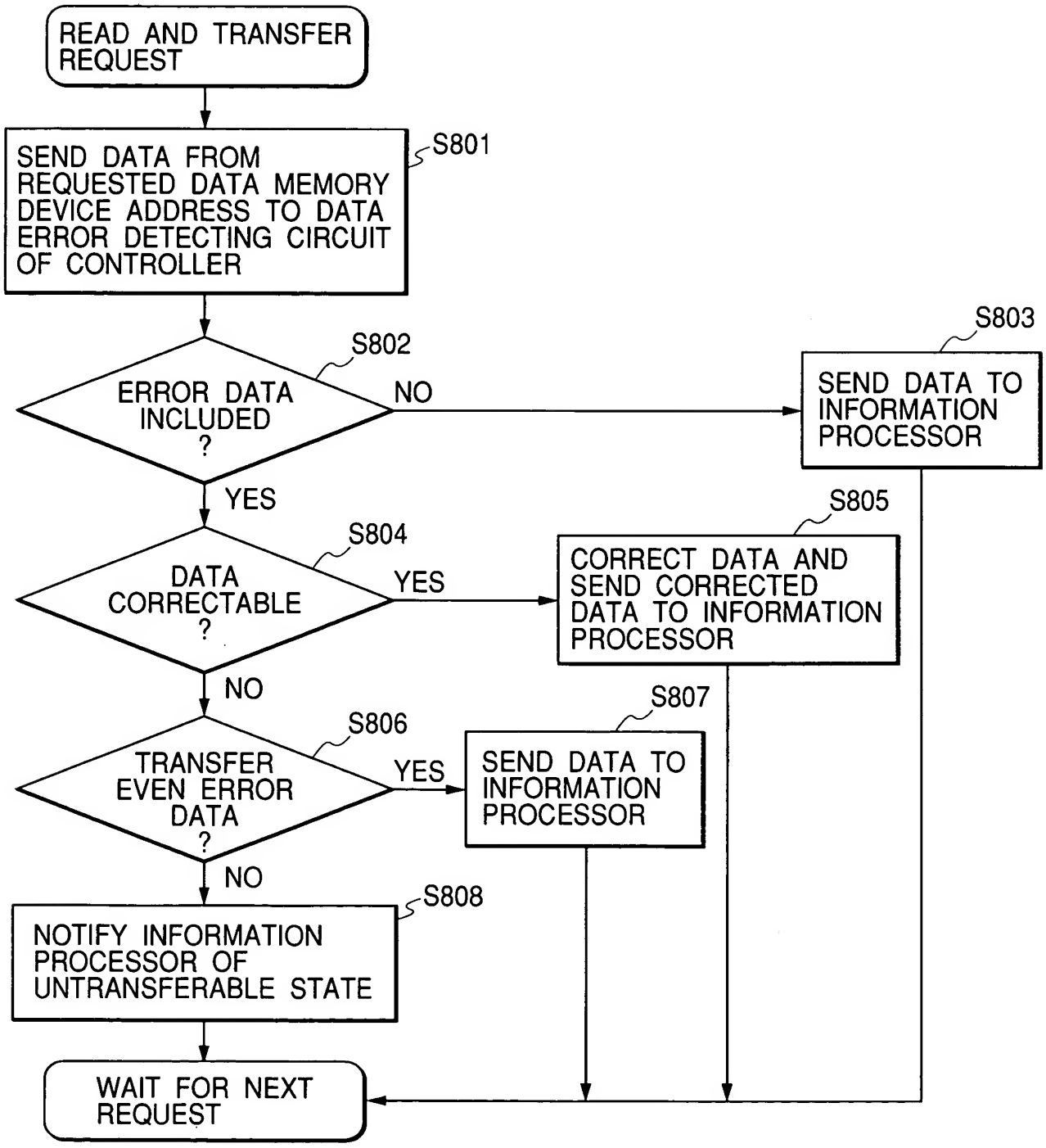

READ AND TRANSFER REQUEST
SEND DATA FROM REQUESTED DATA MEMORY DEVICE ADDRESS TO DATA ERROR DETECTING CIRCUIT OF CONTROLLER
S801
ERROR DATA INCLUDED ?
S802
NO
YES
SEND DATA TO INFORMATION PROCESSOR
S803
DATA CORRECTABLE ?
S804
YES
CORRECT DATA AND SEND CORRECTED DATA TO INFORMATION PROCESSOR
S805
NO
TRANSFER EVEN ERROR DATA ?
S806
YES
SEND DATA TO INFORMATION PROCESSOR
S807
NO
NOTIFY INFORMATION PROCESSOR OF UNTRANSFERABLE STATE
S808
WAIT FOR NEXT REQUEST

FIG. 28

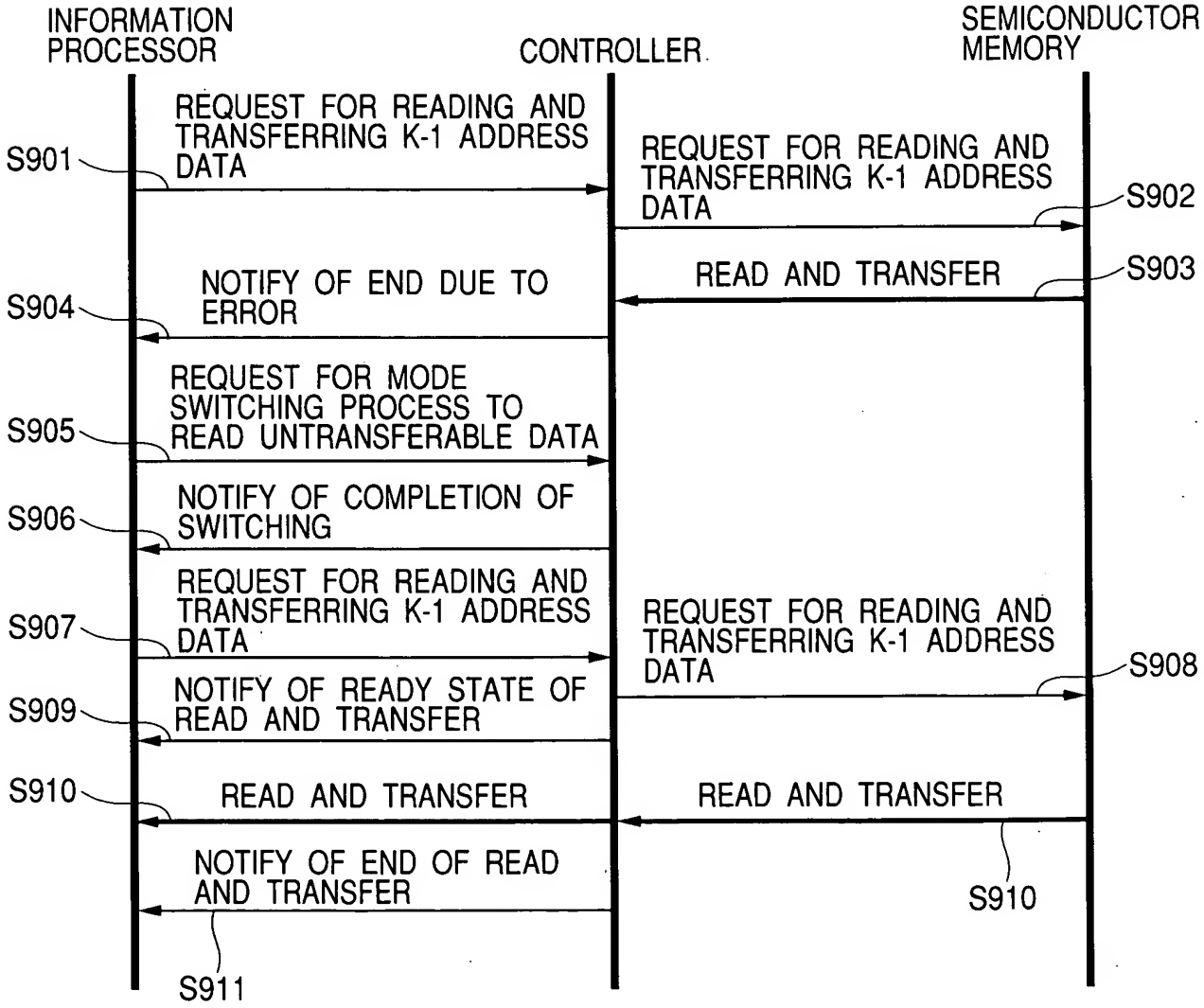

INFORMATION PROCESSOR
CONTROLLER
SEMICONDUCTOR MEMORY
S901
REQUEST FOR READING AND TRANSFERRING K-1 ADDRESS DATA
REQUEST FOR READING AND TRANSFERRING K-1 ADDRESS DATA
S902
READ AND TRANSFER
S903
S904
NOTIFY OF END DUE TO ERROR
S905
REQUEST FOR MODE SWITCHING PROCESS TO READ UNTRANSFERABLE DATA
S906
NOTIFY OF COMPLETION OF SWITCHING
S907
REQUEST FOR READING AND TRANSFERRING K-1 ADDRESS DATA
REQUEST FOR READING AND TRANSFERRING K-1 ADDRESS DATA
S908
S909
NOTIFY OF READY STATE OF READ AND TRANSFER
S910
READ AND TRANSFER
READ AND TRANSFER
NOTIFY OF END OF READ AND TRANSFER
S910
S911

FIG. 29

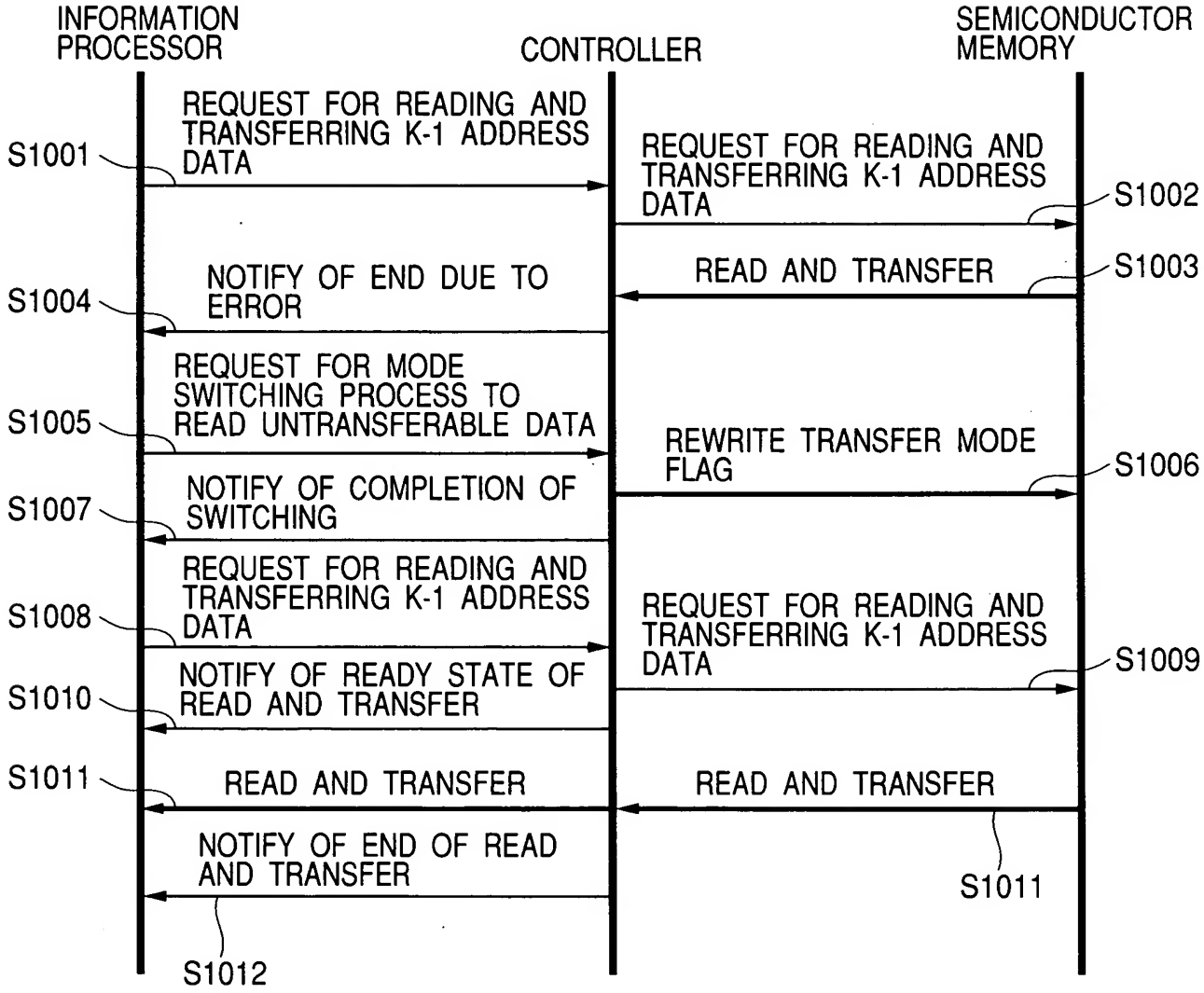

INFORMATION PROCESSOR
CONTROLLER
SEMICONDUCTOR MEMORY
S1001
REQUEST FOR READING AND TRANSFERRING K-1 ADDRESS DATA
REQUEST FOR READING AND TRANSFERRING K-1 ADDRESS DATA
S1002
READ AND TRANSFER
S1003
S1004
NOTIFY OF END DUE TO ERROR
S1005
REQUEST FOR MODE SWITCHING PROCESS TO READ UNTRANSFERABLE DATA
REWRITE TRANSFER MODE FLAG
S1006
S1007
NOTIFY OF COMPLETION OF SWITCHING
S1008
REQUEST FOR READING AND TRANSFERRING K-1 ADDRESS DATA
REQUEST FOR READING AND TRANSFERRING K-1 ADDRESS DATA
S1009
S1010
NOTIFY OF READY STATE OF READ AND TRANSFER
S1011
READ AND TRANSFER
READ AND TRANSFER
NOTIFY OF END OF READ AND TRANSFER
S1011
S1012

FIG. 30

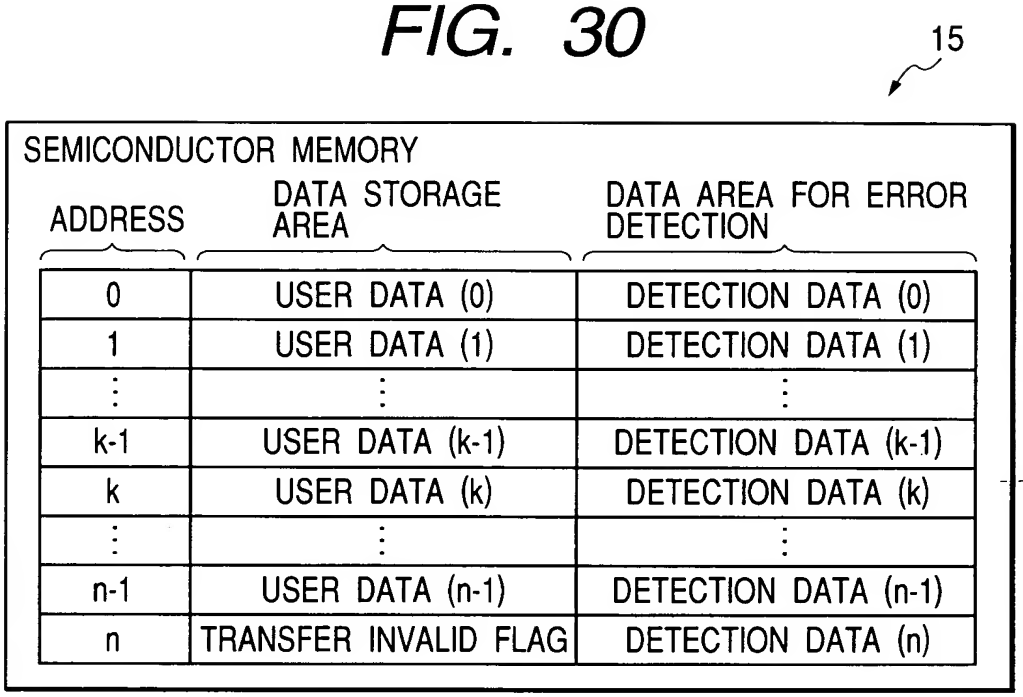

15
SEMICONDUCTOR MEMORY
ADDRESS
DATA STORAGE AREA
DATA AREA FOR ERROR DETECTION
0
USER DATA (0)
DETECTION DATA (0)
1
USER DATA (1)
DETECTION DATA (1)
k-1
USER DATA (k-1)
DETECTION DATA (k-1)
k
USER DATA (k)
DETECTION DATA (k)
n-1
USER DATA (n-1)
DETECTION DATA (n-1)
n
TRANSFER INVALID FLAG
DETECTION DATA (n)

FIG. 31

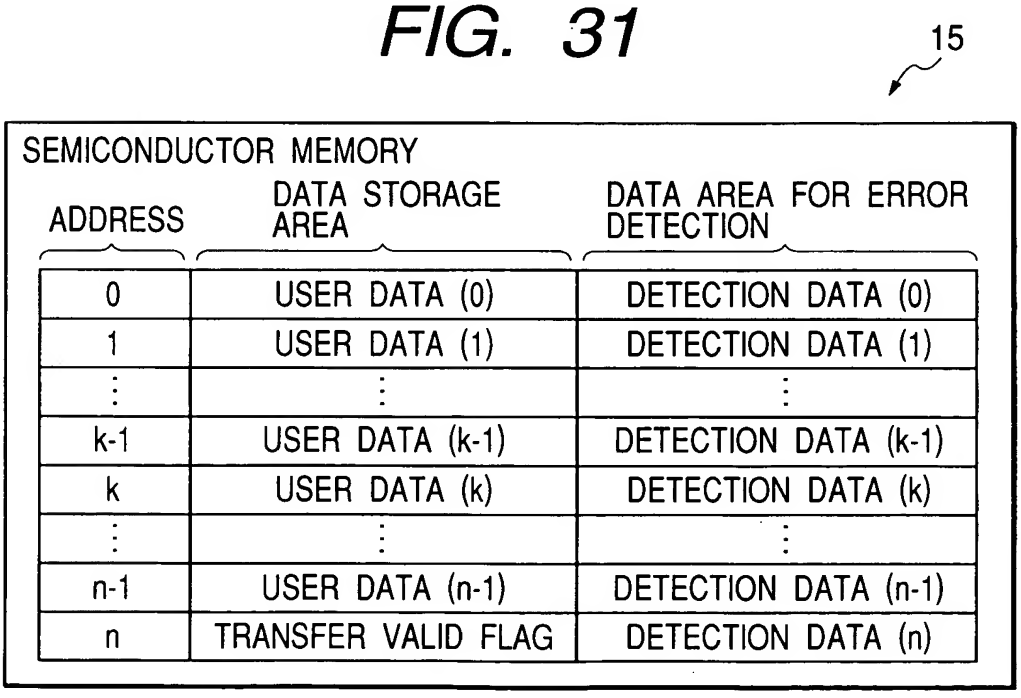

15
SEMICONDUCTOR MEMORY
ADDRESS
DATA STORAGE AREA
DATA AREA FOR ERROR DETECTION
0
USER DATA (0)
DETECTION DATA (0)
1
USER DATA (1)
DETECTION DATA (1)
k-1
USER DATA (k-1)
DETECTION DATA (k-1)
k
USER DATA (k)
DETECTION DATA (k)
n-1
USER DATA (n-1)
DETECTION DATA (n-1)
n
TRANSFER VALID FLAG
DETECTION DATA (n)

FIG. 32

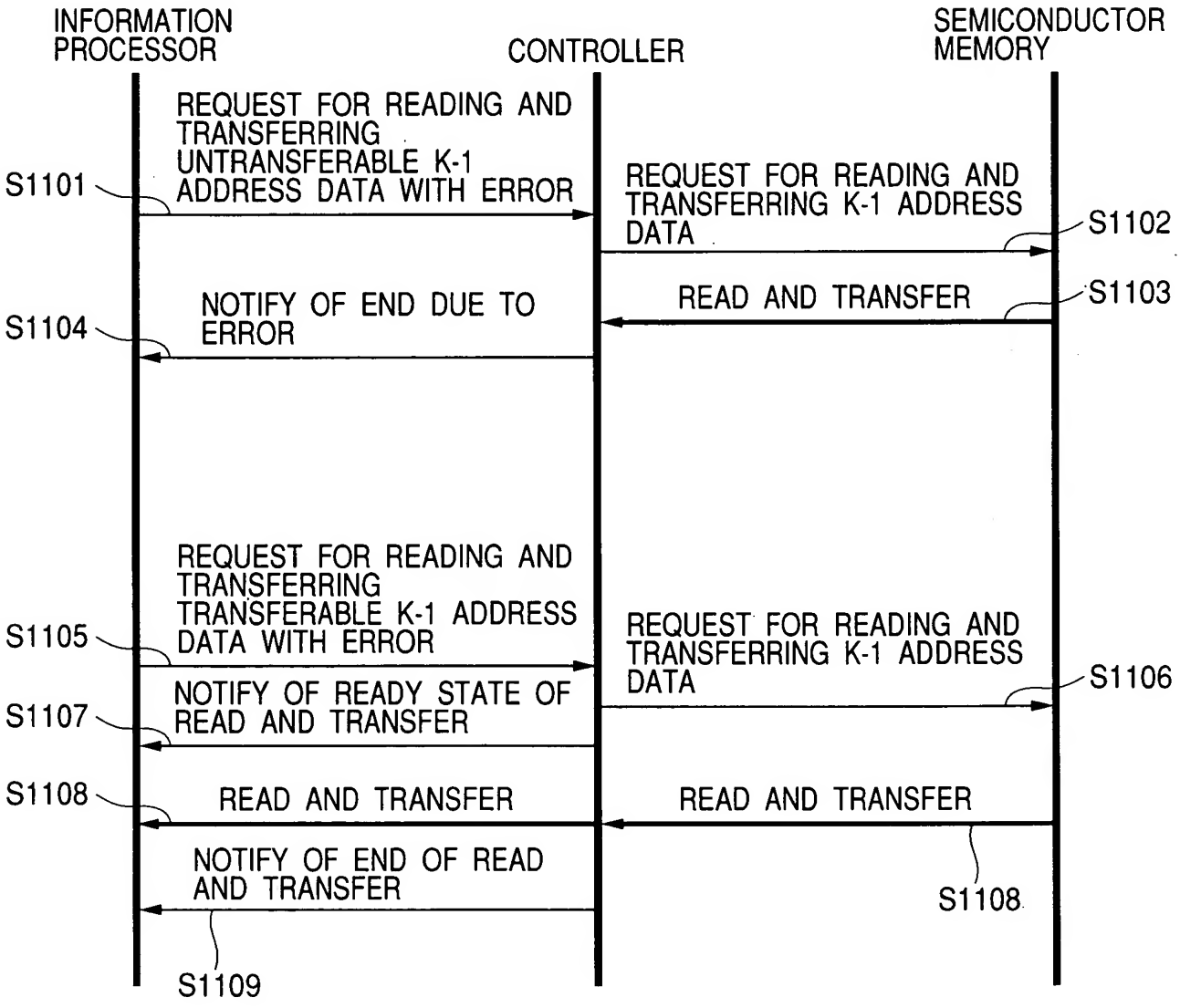
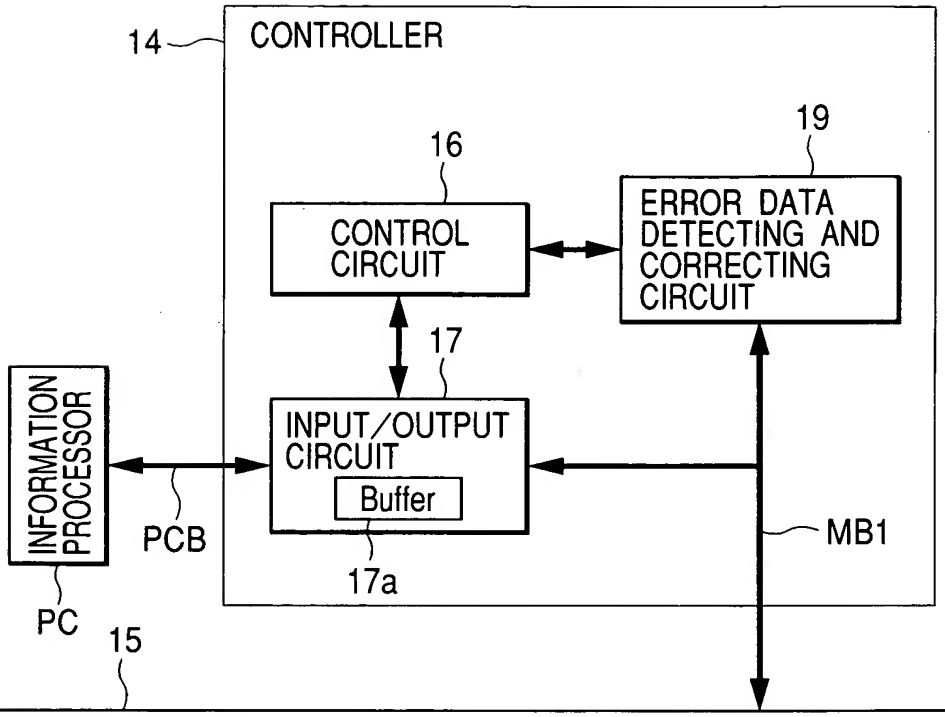

INFORMATION PROCESSOR
CONTROLLER
SEMICONDUCTOR MEMORY
S1101
REQUEST FOR READING AND TRANSFERRING UNTRANSFERABLE K-1 ADDRESS DATA WITH ERROR
REQUEST FOR READING AND TRANSFERRING K-1 ADDRESS DATA
S1102
READ AND TRANSFER
S1103
S1104
NOTIFY OF END DUE TO ERROR
REQUEST FOR READING AND TRANSFERRING TRANSFERABLE K-1 ADDRESS DATA WITH ERROR
S1105
REQUEST FOR READING AND TRANSFERRING K-1 ADDRESS DATA
S1106
S1107
NOTIFY OF READY STATE OF READ AND TRANSFER
S1108
READ AND TRANSFER
READ AND TRANSFER
NOTIFY OF END OF READ AND TRANSFER
S1108
S1109

FIG. 33



SEMICONDUCTOR MEMORY

ADDRESS	DATA STORAGE AREA	TRANSFER FLAG	DATA AREA FOR ERROR DETECTION
0	USER DATA (0)	ERROR DATA UNTRANSFERABLE	DETECTION DATA (0)
1	USER DATA (1)	ERROR DATA UNTRANSFERABLE	DETECTION DATA (1)
⋮	⋮		⋮
k-1	USER DATA (k-1)	ERROR DATA UNTRANSFERABLE	DETECTION DATA (k-1)
k	USER DATA (k)	ERROR DATA TRANSFERABLE	DETECTION DATA (k)
⋮	⋮		⋮
n-1	USER DATA (n-1)	ERROR DATA UNTRANSFERABLE	DETECTION DATA (n-1)

FIG. 34

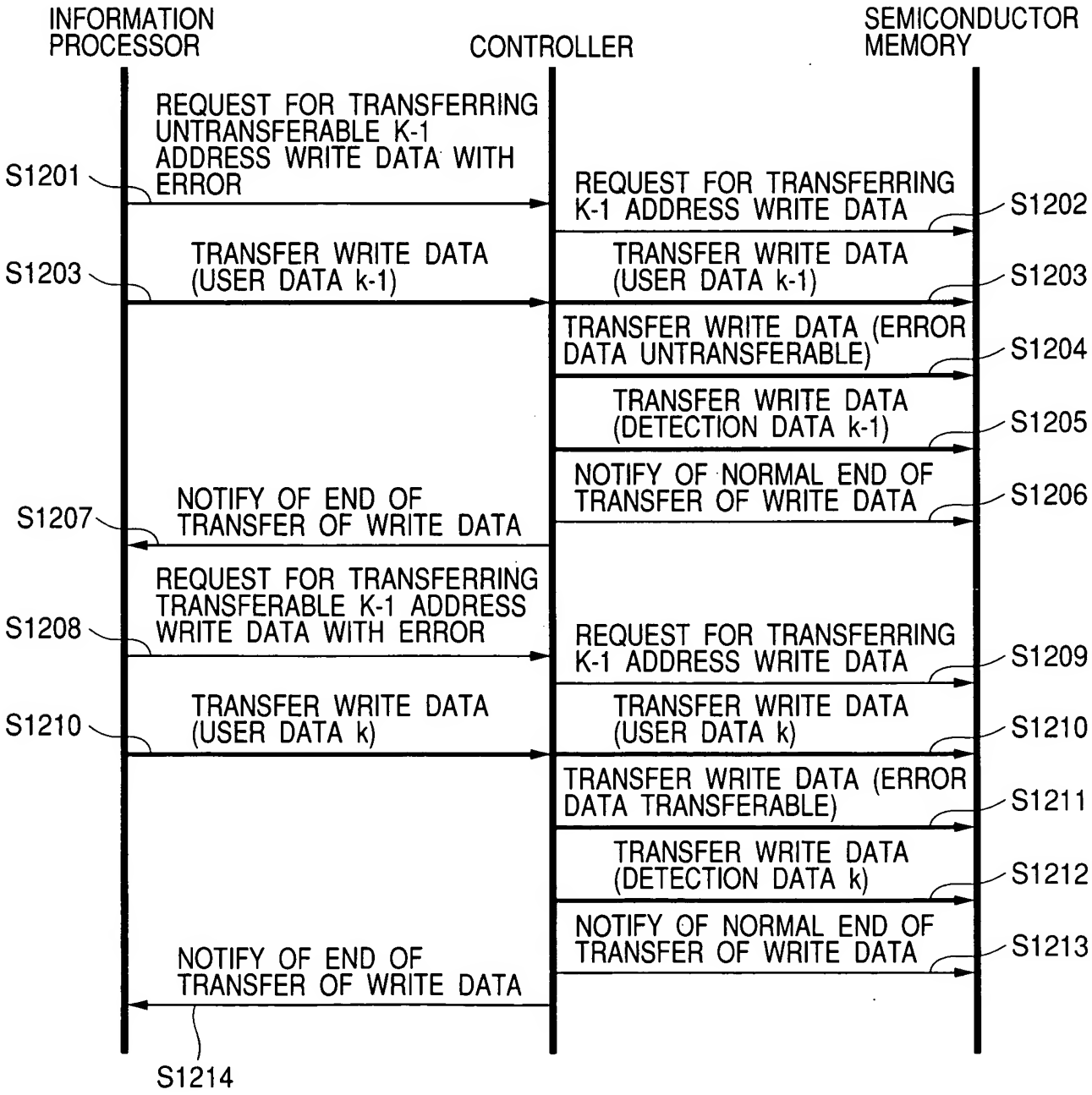

INFORMATION PROCESSOR
CONTROLLER
SEMICONDUCTOR MEMORY
REQUEST FOR TRANSFERRING UNTRANSFERABLE K-1 ADDRESS WRITE DATA WITH ERROR
S1201
REQUEST FOR TRANSFERRING K-1 ADDRESS WRITE DATA
S1202
TRANSFER WRITE DATA (USER DATA k-1)
S1203
TRANSFER WRITE DATA (USER DATA k-1)
S1203
TRANSFER WRITE DATA (ERROR DATA UNTRANSFERABLE)
S1204
TRANSFER WRITE DATA (DETECTION DATA k-1)
S1205
NOTIFY OF NORMAL END OF TRANSFER OF WRITE DATA
S1206
NOTIFY OF END OF TRANSFER OF WRITE DATA
S1207
REQUEST FOR TRANSFERRING TRANSFERABLE K-1 ADDRESS WRITE DATA WITH ERROR
S1208
REQUEST FOR TRANSFERRING K-1 ADDRESS WRITE DATA
S1209
TRANSFER WRITE DATA (USER DATA k)
S1210
TRANSFER WRITE DATA (USER DATA k)
S1210
TRANSFER WRITE DATA (ERROR DATA TRANSFERABLE)
S1211
TRANSFER WRITE DATA (DETECTION DATA k)
S1212
NOTIFY OF NORMAL END OF TRANSFER OF WRITE DATA
S1213
NOTIFY OF END OF TRANSFER OF WRITE DATA
S1214

FIG. 35

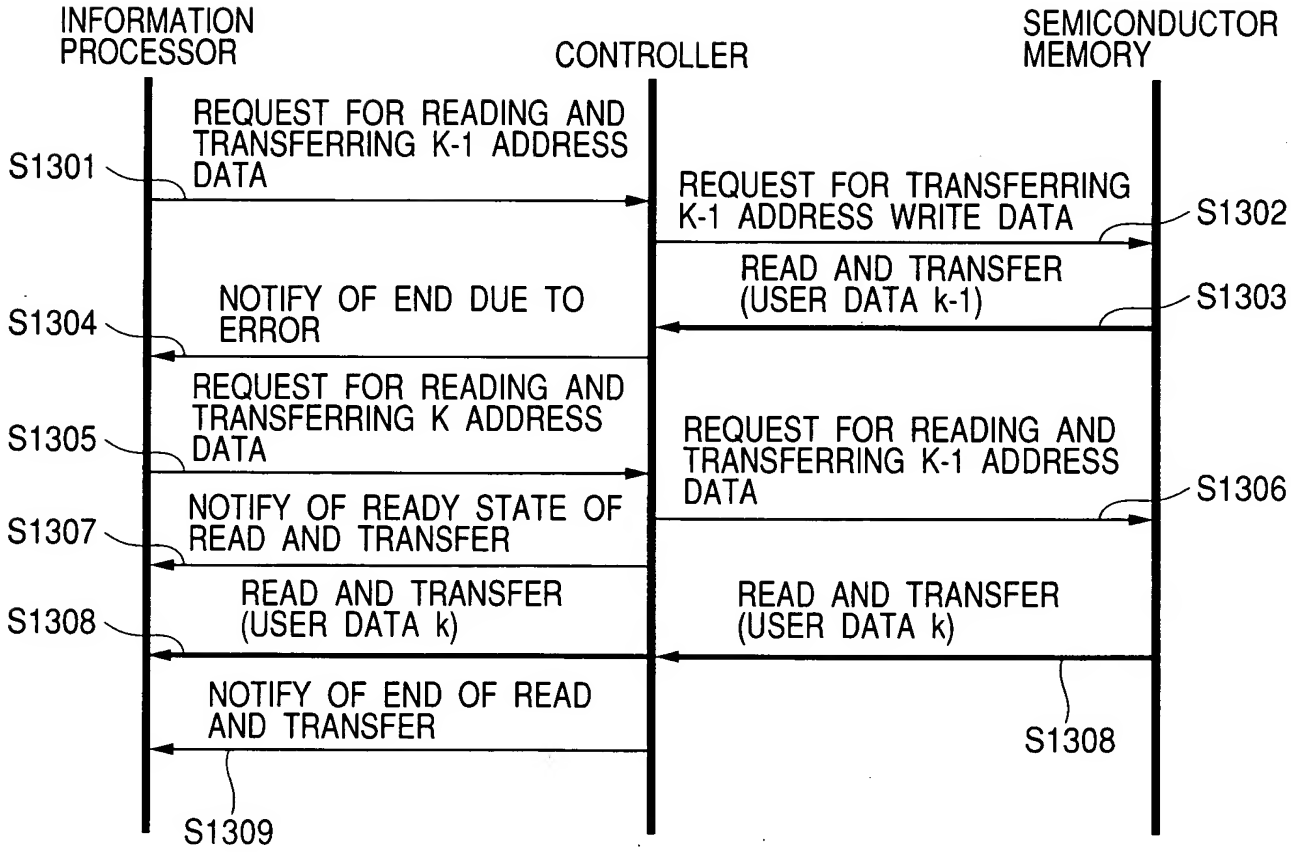
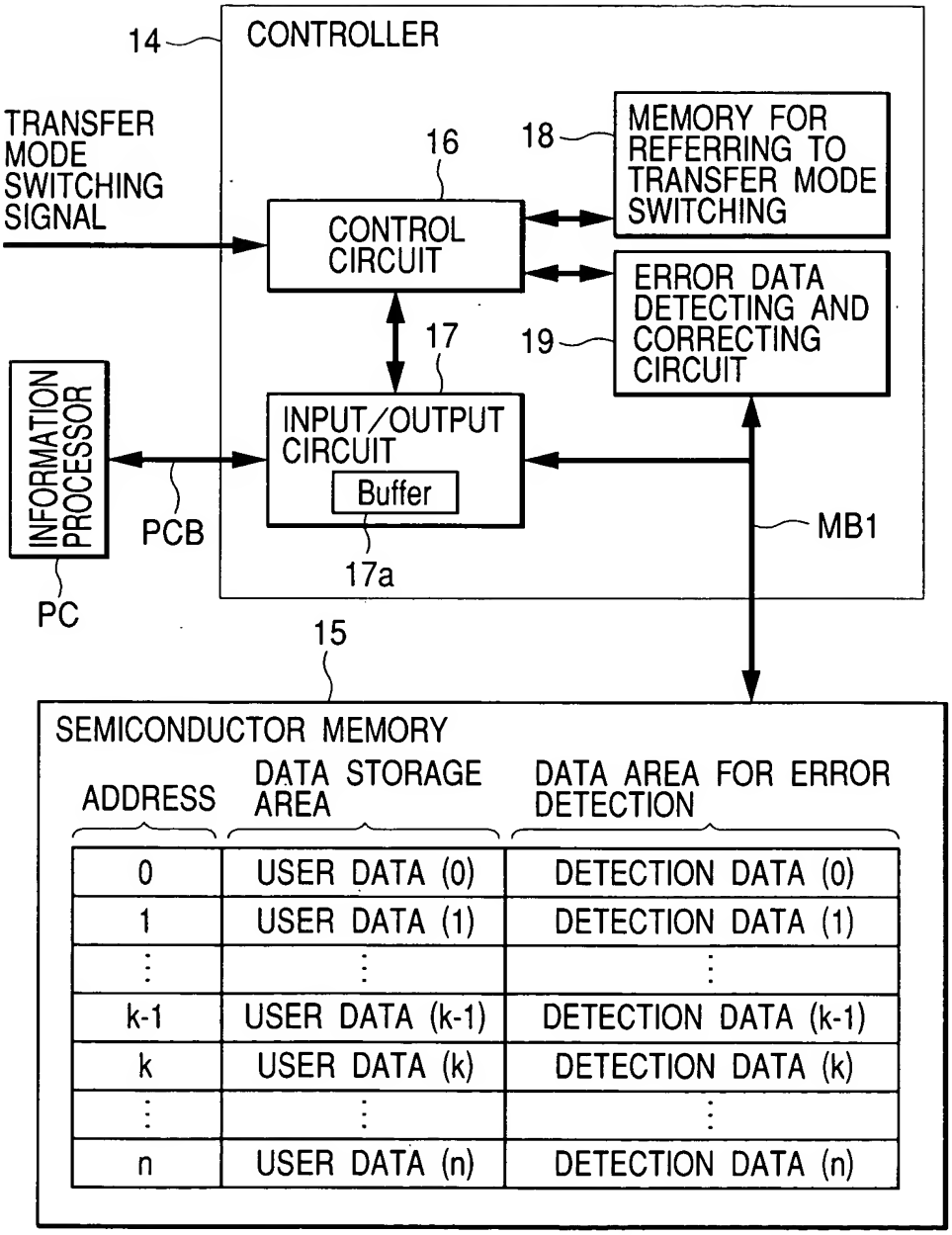

INFORMATION PROCESSOR
CONTROLLER
SEMICONDUCTOR MEMORY
S1301
REQUEST FOR READING AND TRANSFERRING K-1 ADDRESS DATA
REQUEST FOR TRANSFERRING K-1 ADDRESS WRITE DATA
S1302
READ AND TRANSFER (USER DATA k-1)
S1303
S1304
NOTIFY OF END DUE TO ERROR
S1305
REQUEST FOR READING AND TRANSFERRING K ADDRESS DATA
REQUEST FOR READING AND TRANSFERRING K-1 ADDRESS DATA
S1306
S1307
NOTIFY OF READY STATE OF READ AND TRANSFER
S1308
READ AND TRANSFER (USER DATA k)
READ AND TRANSFER (USER DATA k)
NOTIFY OF END OF READ AND TRANSFER
S1308
S1309

FIG. 36


14
CONTROLLER
TRANSFER MODE SWITCHING SIGNAL
16
18
MEMORY FOR REFERRING TO TRANSFER MODE SWITCHING
CONTROL CIRCUIT
ERROR DATA DETECTING AND CORRECTING CIRCUIT
17
19
INFORMATION PROCESSOR
INPUT/OUTPUT CIRCUIT
Buffer
PCB
MB1
17a
PC
15
SEMICONDUCTOR MEMORY
ADDRESS
DATA STORAGE AREA
DATA AREA FOR ERROR DETECTION
0
USER DATA (0)
DETECTION DATA (0)
1
USER DATA (1)
DETECTION DATA (1)
k-1
USER DATA (k-1)
DETECTION DATA (k-1)
k
USER DATA (k)
DETECTION DATA (k)
n
USER DATA (n)
DETECTION DATA (n)